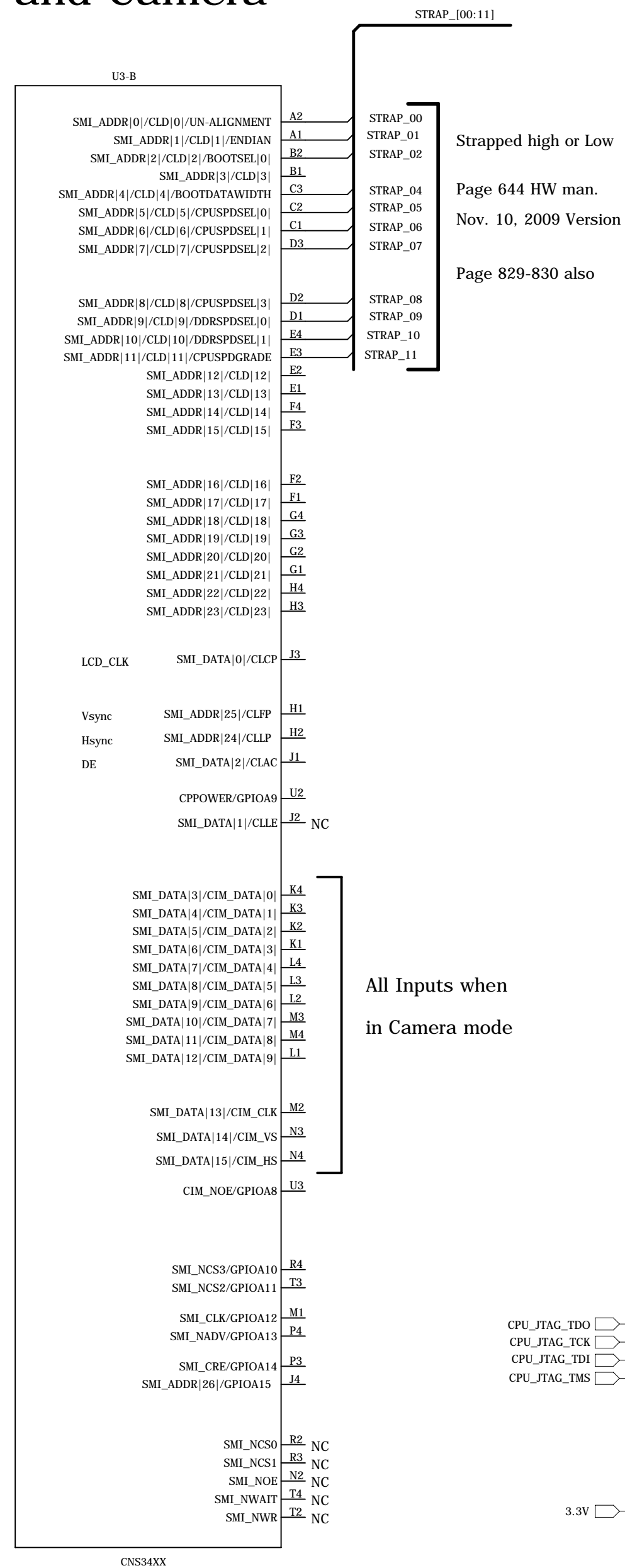
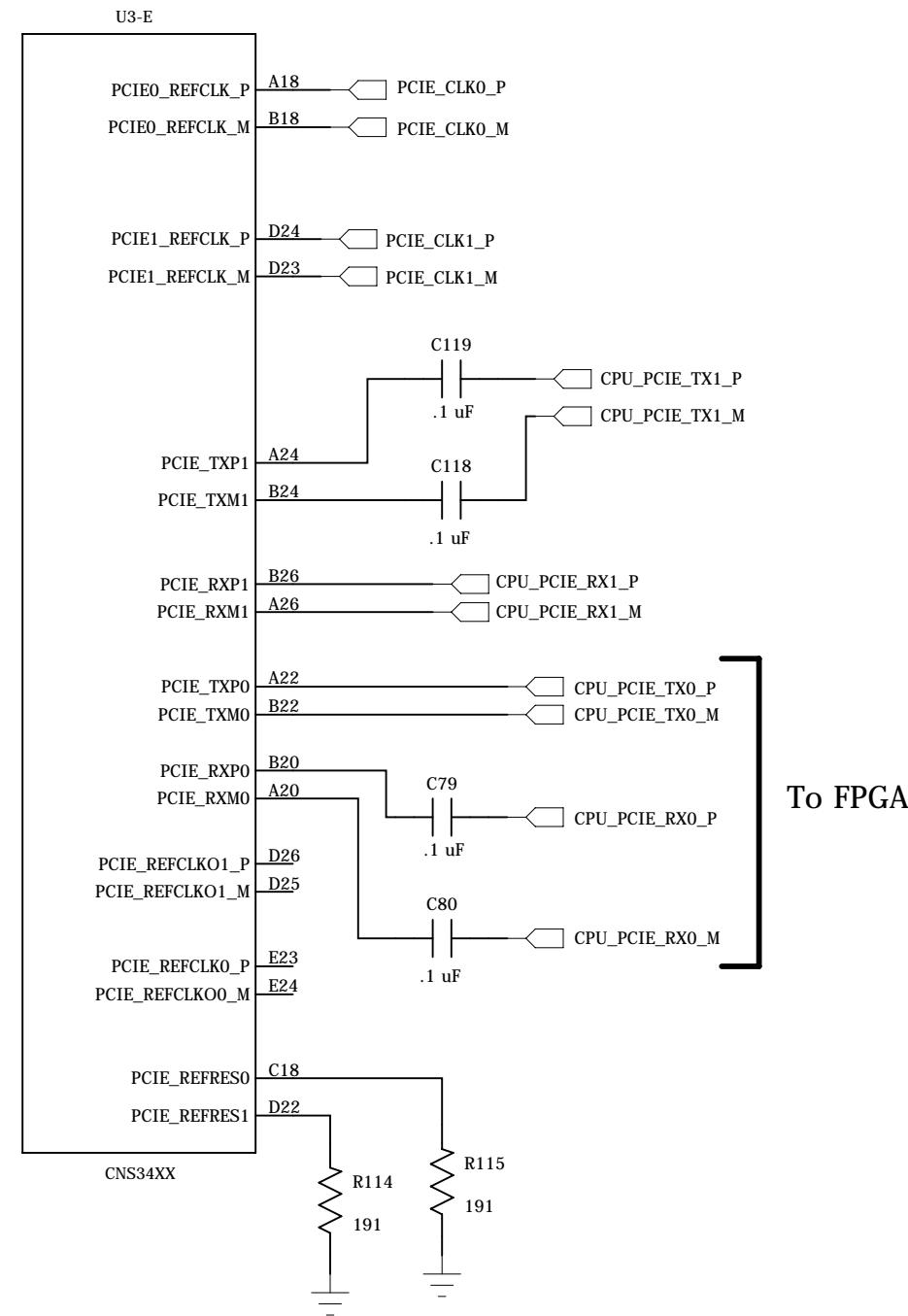


Cavium ARM11 CPU

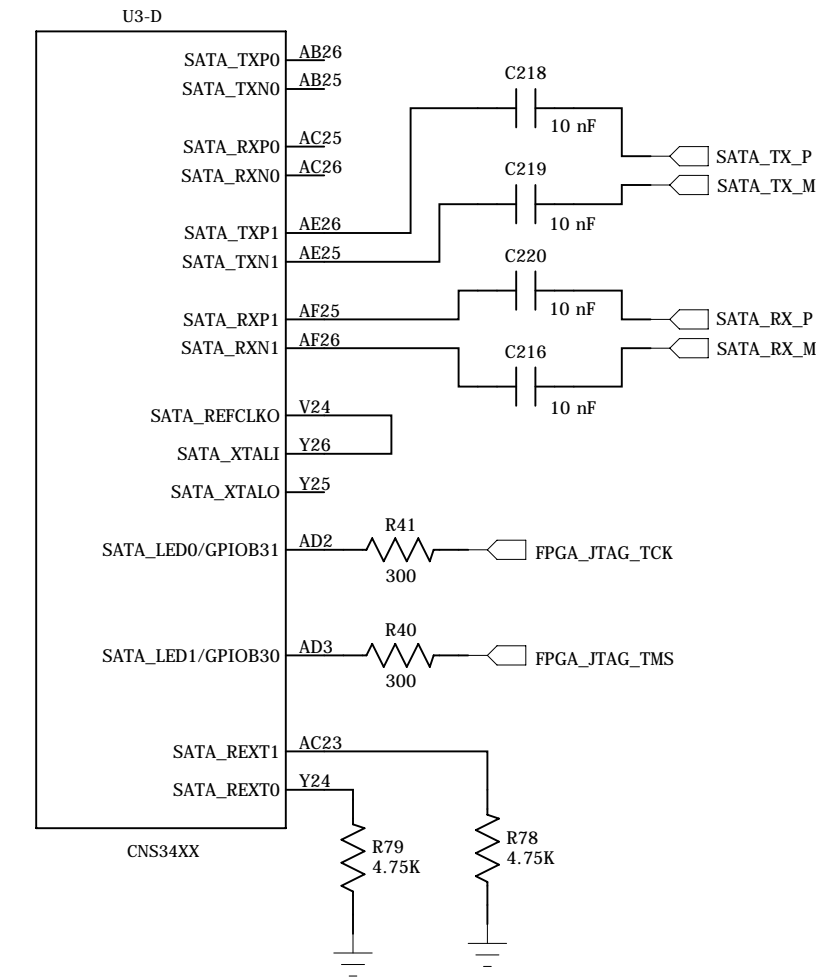
LCD and Camera



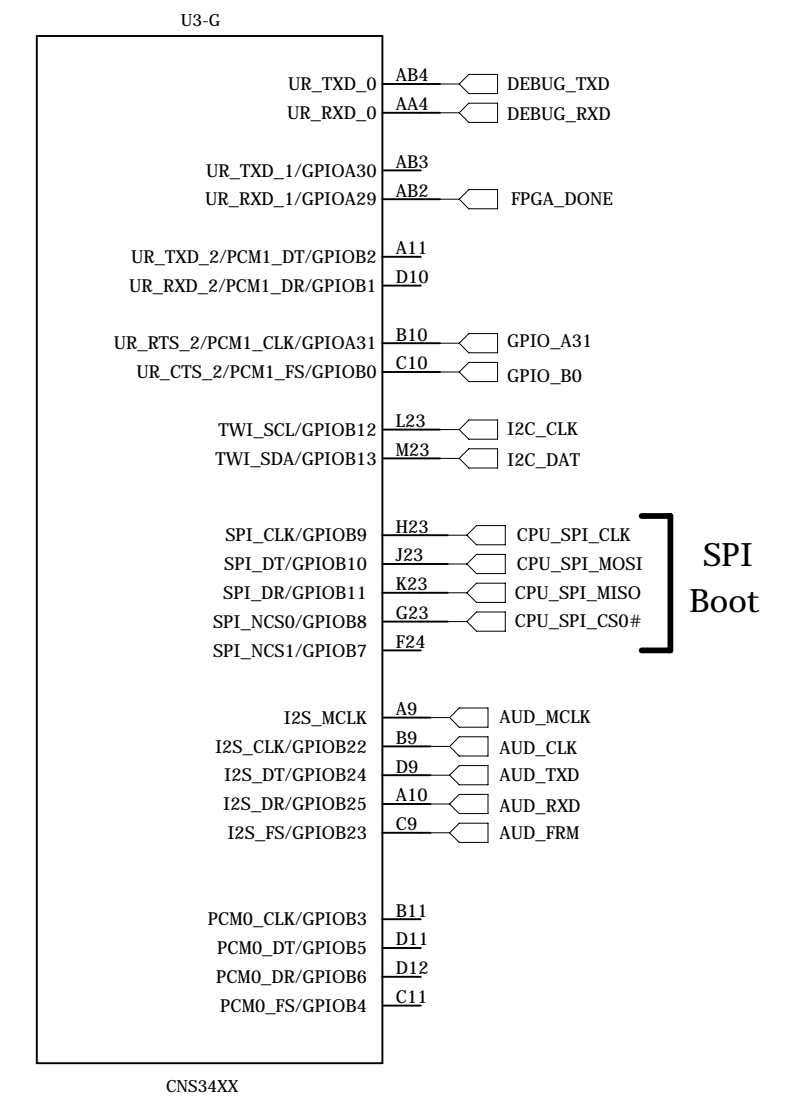
PCI Ex.



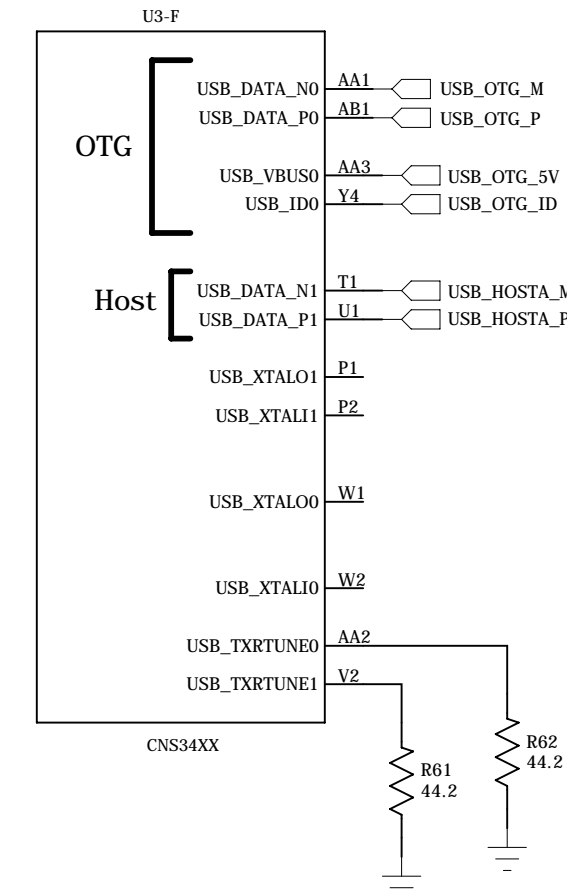
SATA



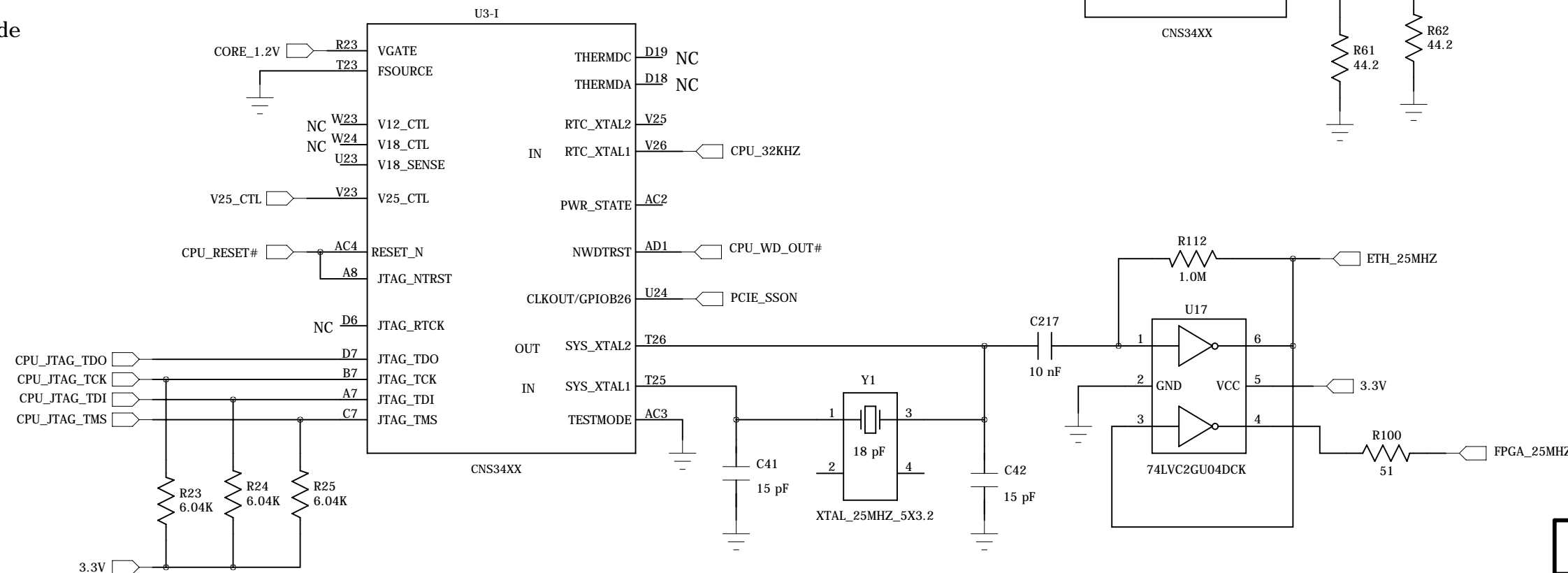
UARTs, SPI I2C, Audio



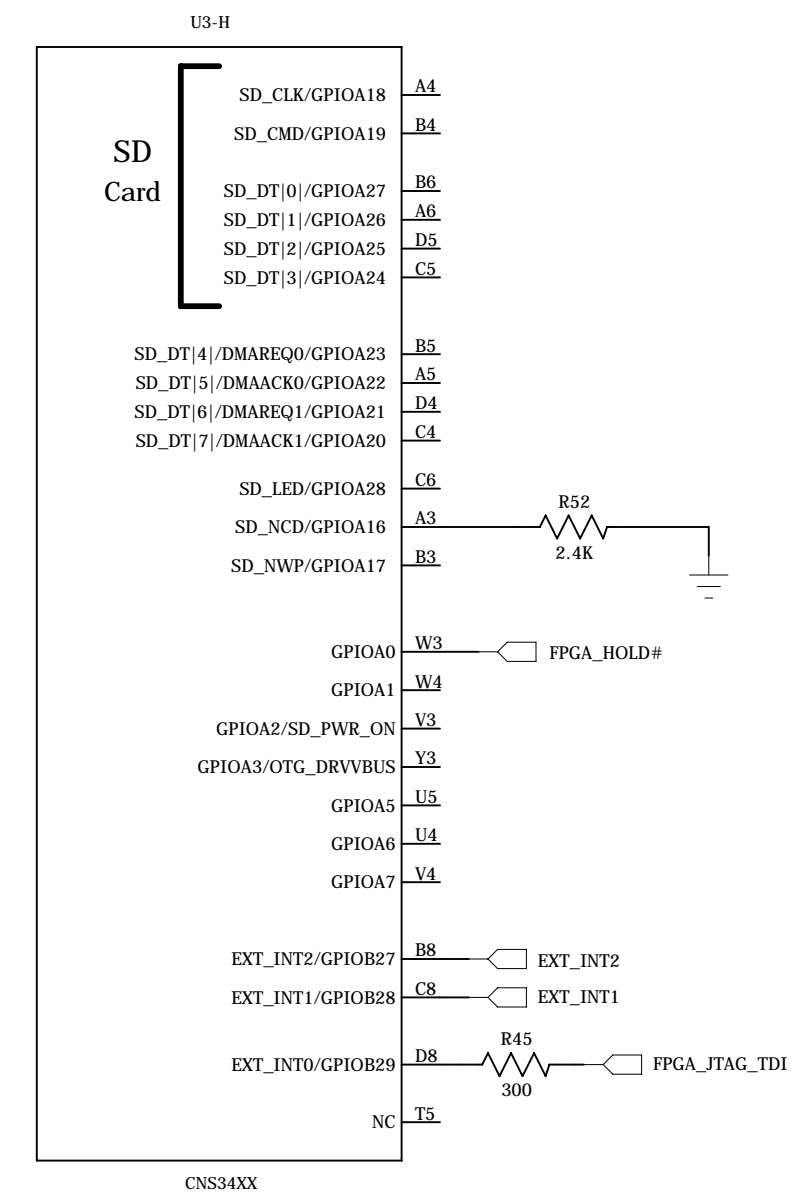
USB



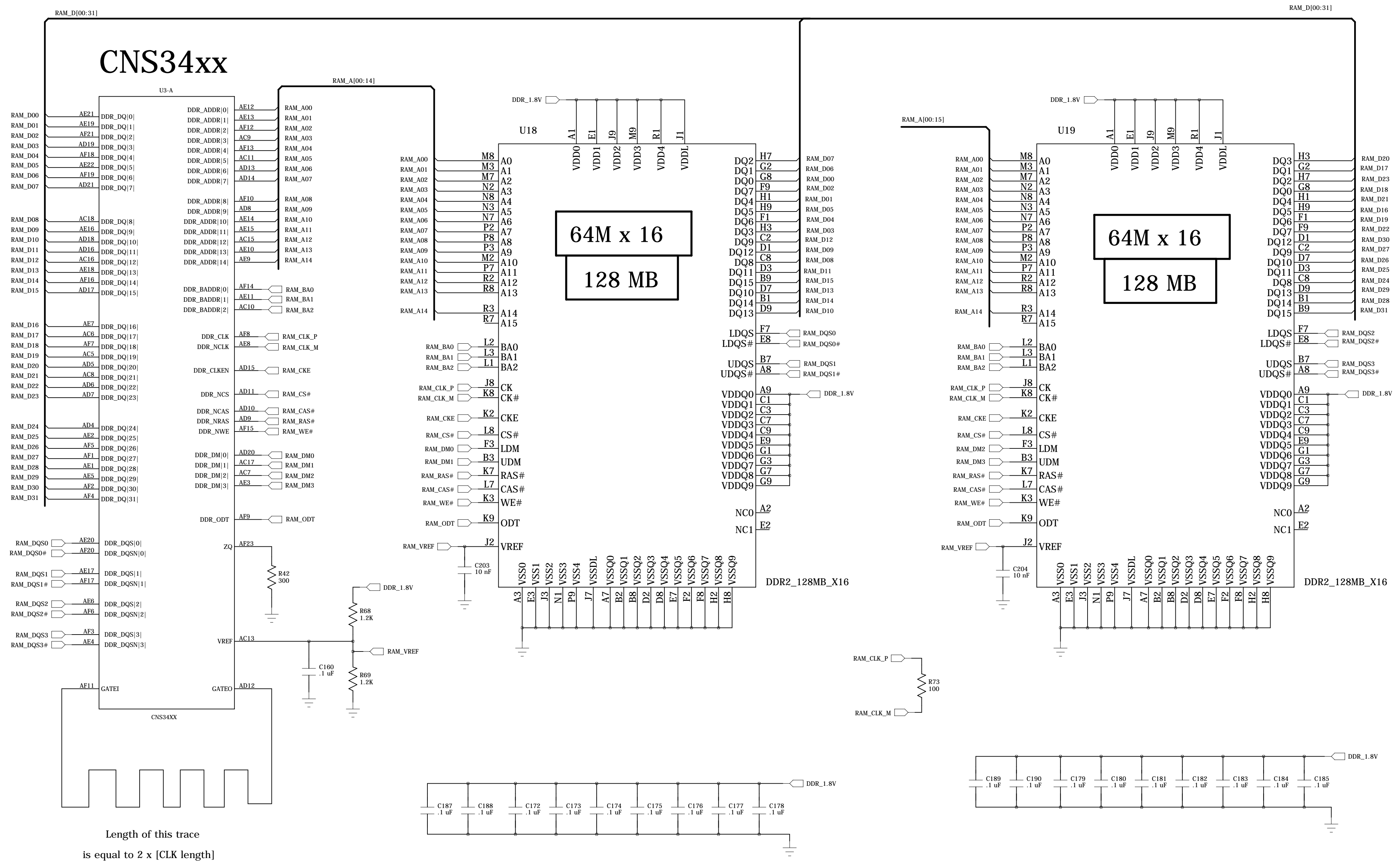
Control



SD Card

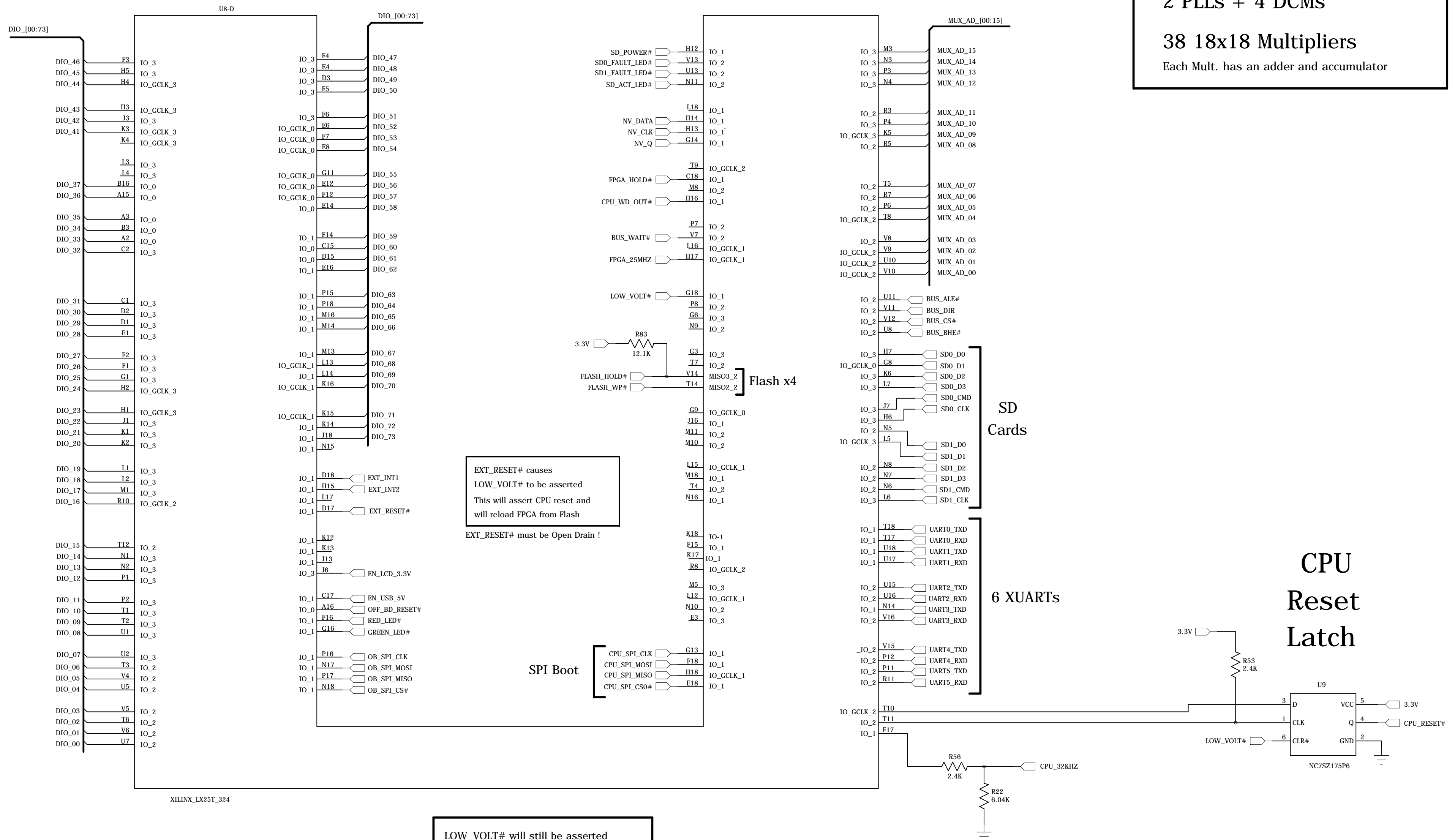


DDR2 SDRAM (256 MByte)



Xilinx LX25T_324 FPGA

25K equivalent LUTs
 15K 6-input LUTs
 30K Flip-flops
 52 [2K x 9] Block RAM
 2 PLLs + 4 DCMs
 38 18x18 Multipliers
 Each Mult. has an adder and accumulator



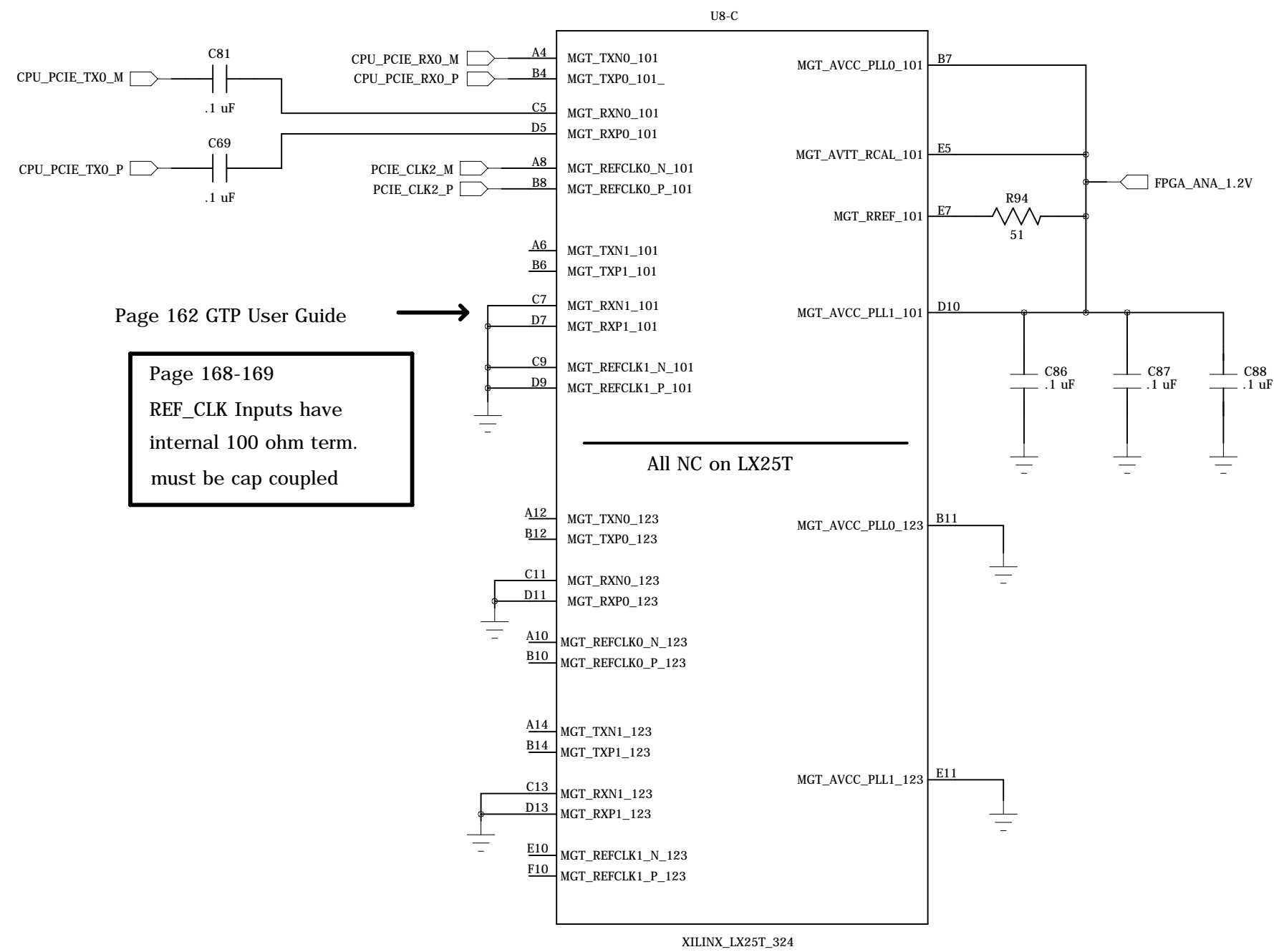
EXT_RESET# causes
 LOW_VOLT# to be asserted
 This will assert CPU reset and
 will reload FPGA from Flash
 EXT_RESET# must be Open Drain !

LOW_VOLT# will still be asserted
 after FPGA is configured
 and can be used as a FPGA reset

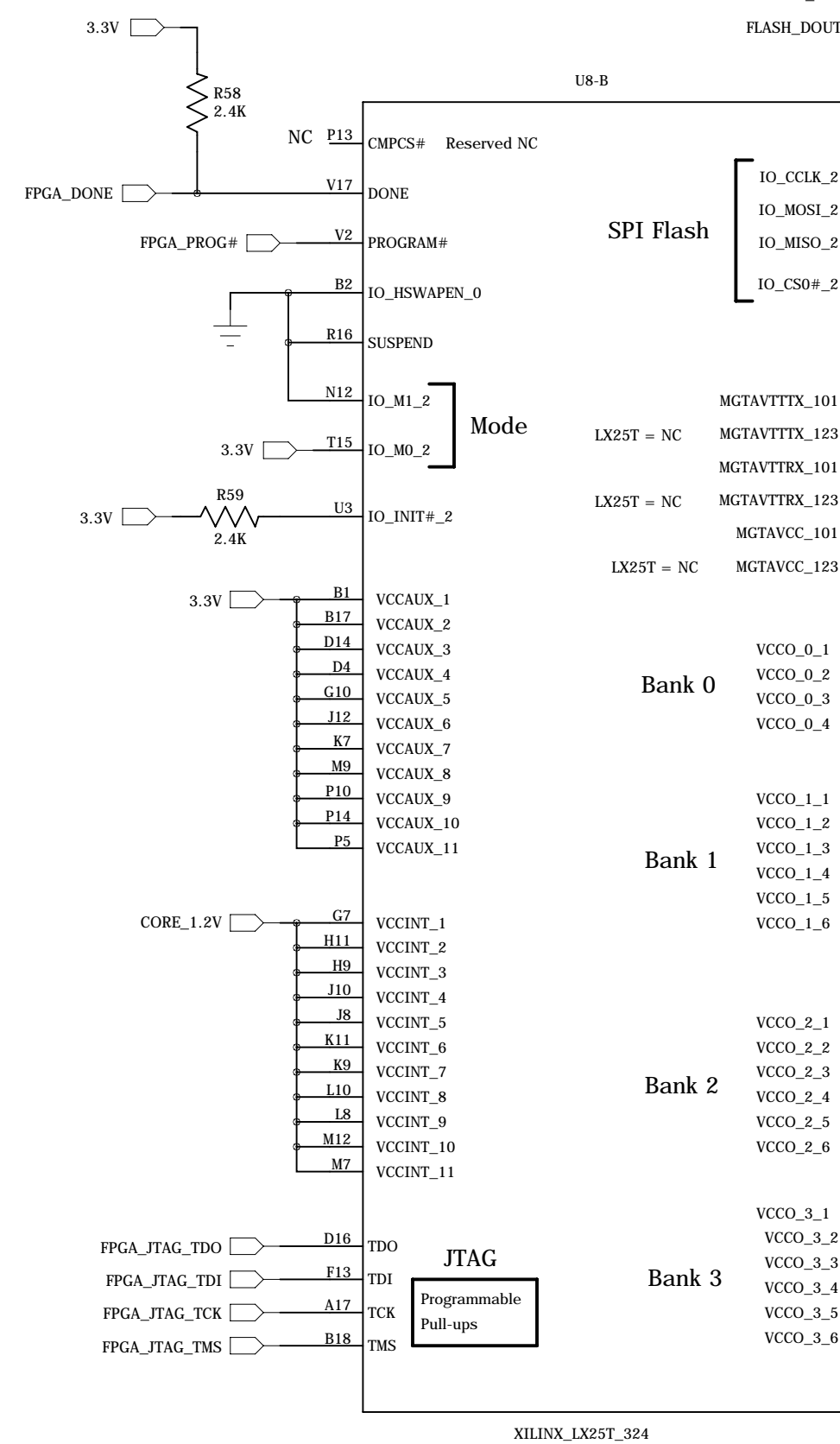
FPGA_HOLD# is driven by CPU and
 can be used as a FPGA reset when
 CPU is doing a soft FPGA reload

Xilinx LX25T_324 FPGA

Gigabit Transceivers

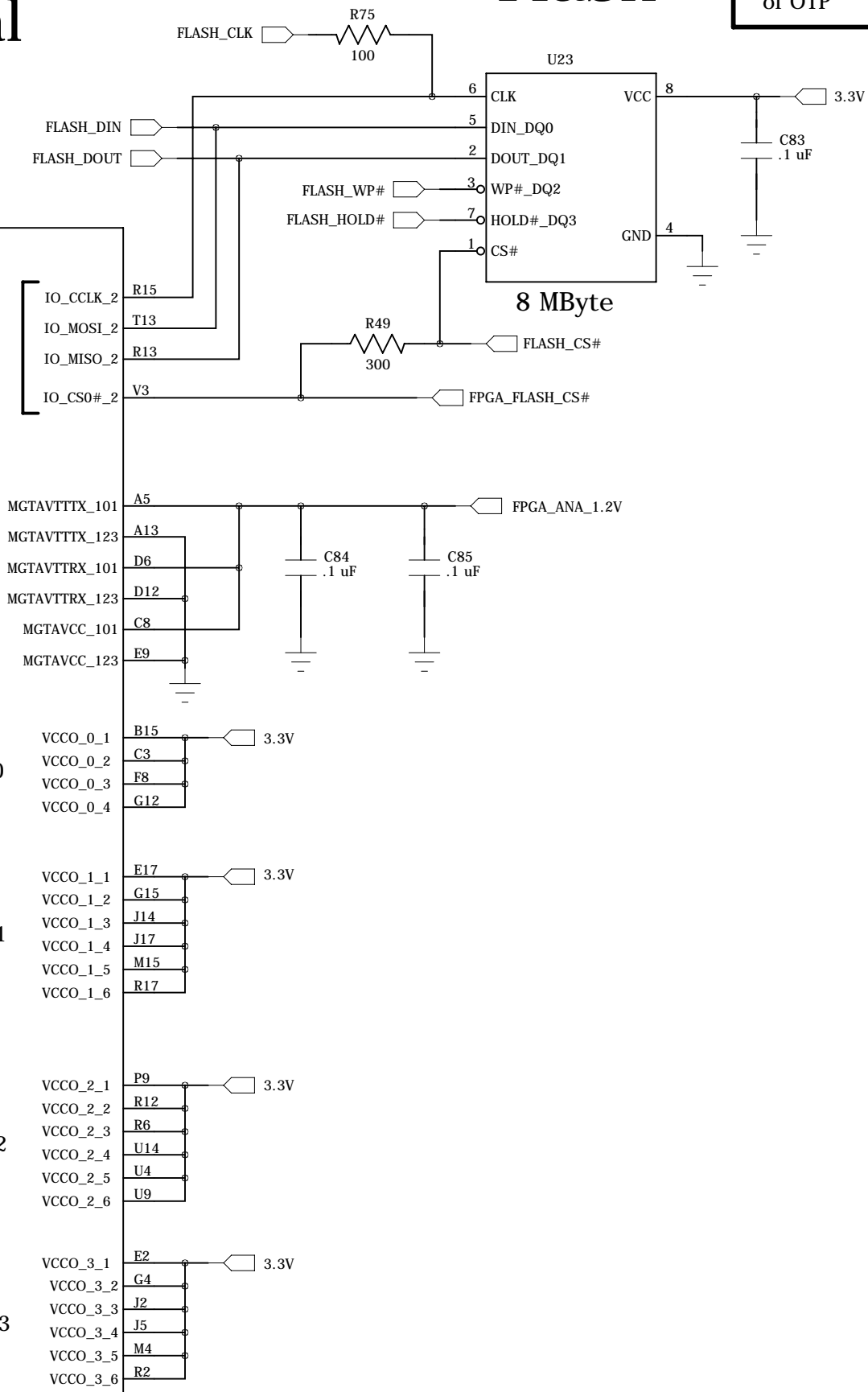


Power and Special Functions

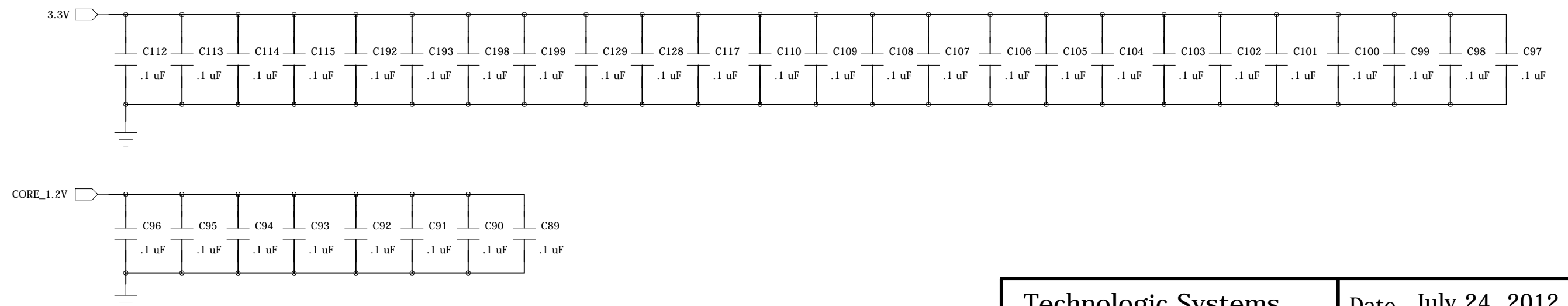
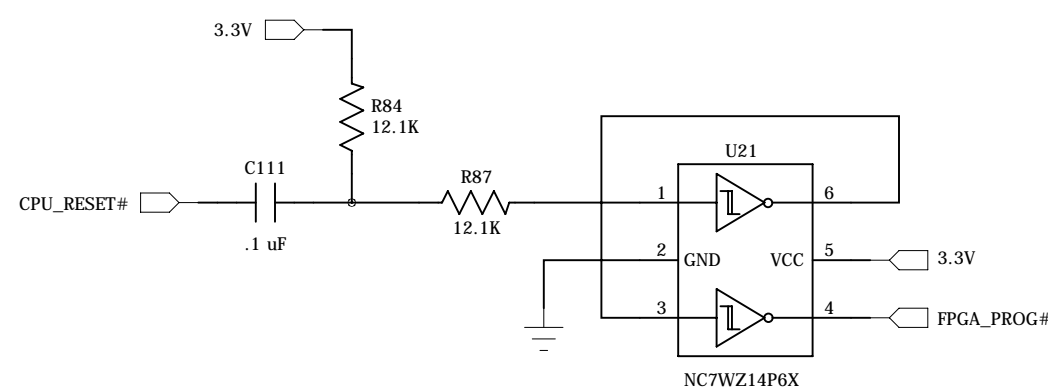


8MB SPI Flash

64 bytes of OTP

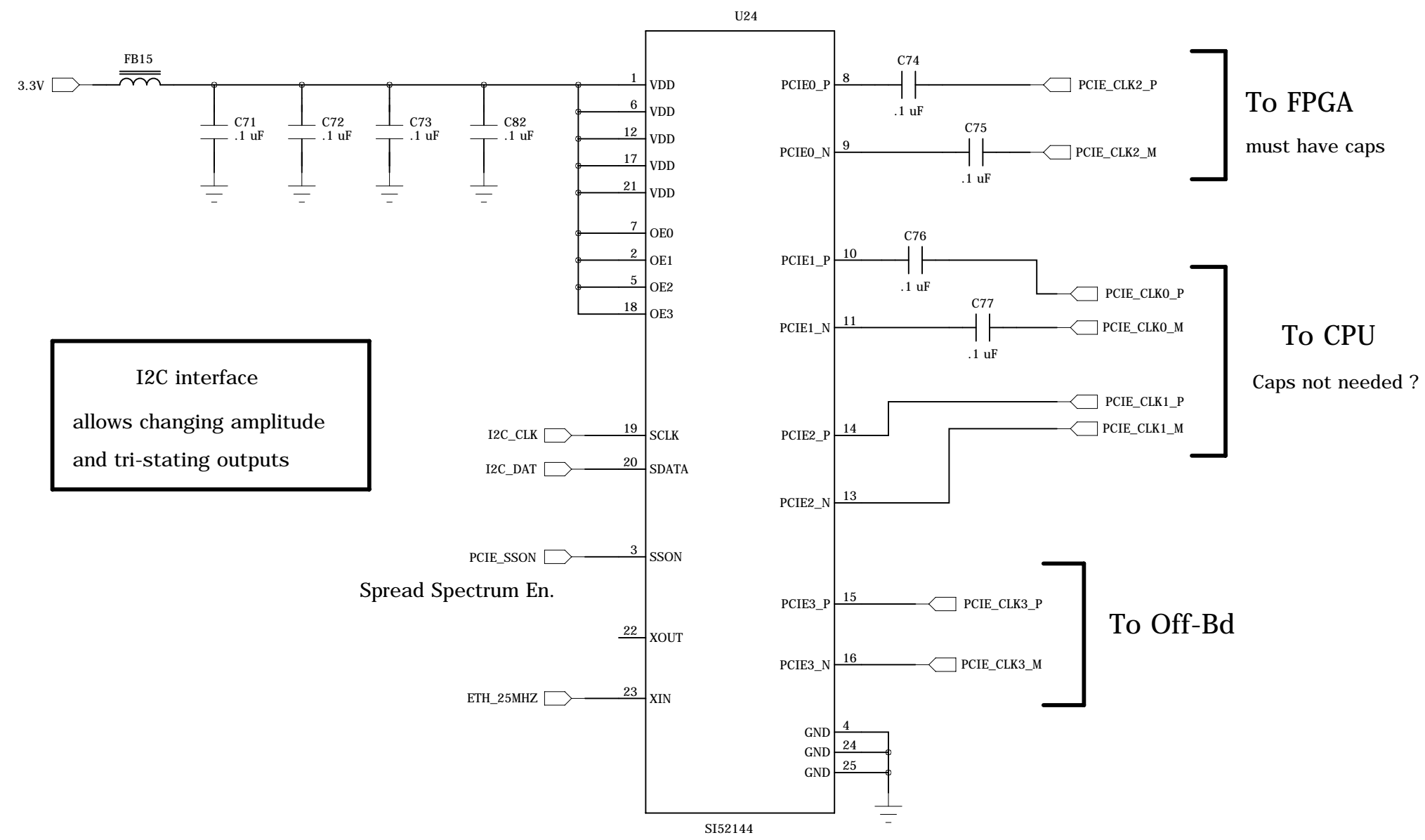


FPGA Reload

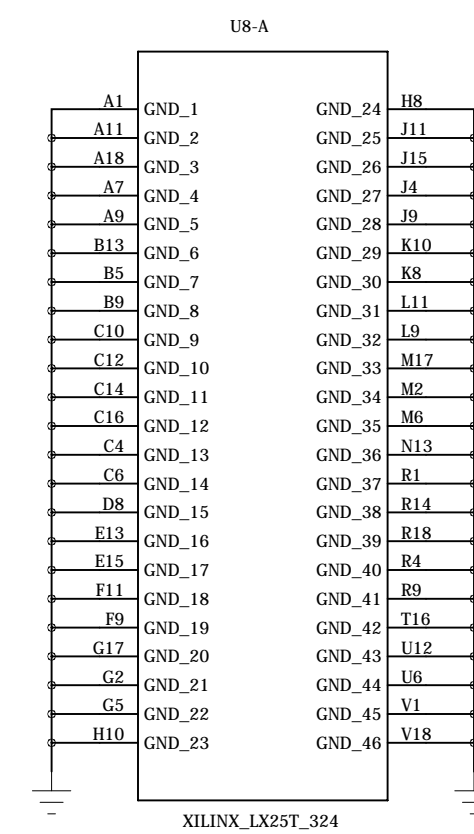


Technologic Systems		Date July 24, 2012	
Title: TS-4300 FPGA			
Rev: B	Designer	Sheet 5 of 10	

PCIe 100 MHz Clock Generator

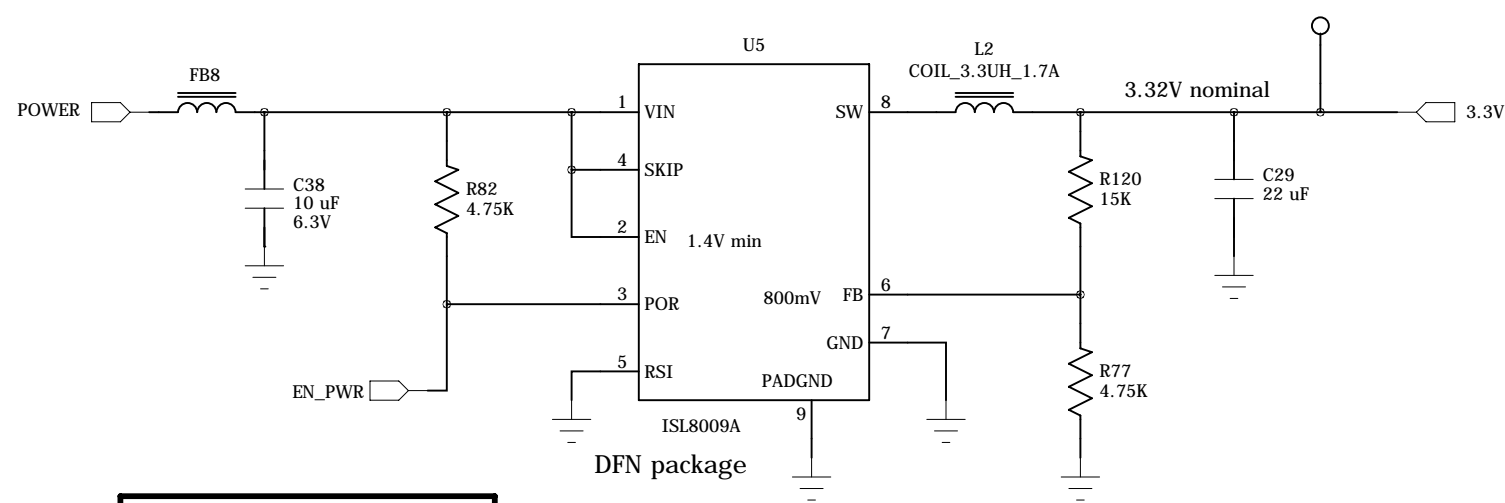


FPGA GND



3.3V Power Supply

up to 1500 mA



EN_PWR goes low when 3.3V out of regulation

Coil = LQH44PN3R3

Max. current = 1.7 Amps

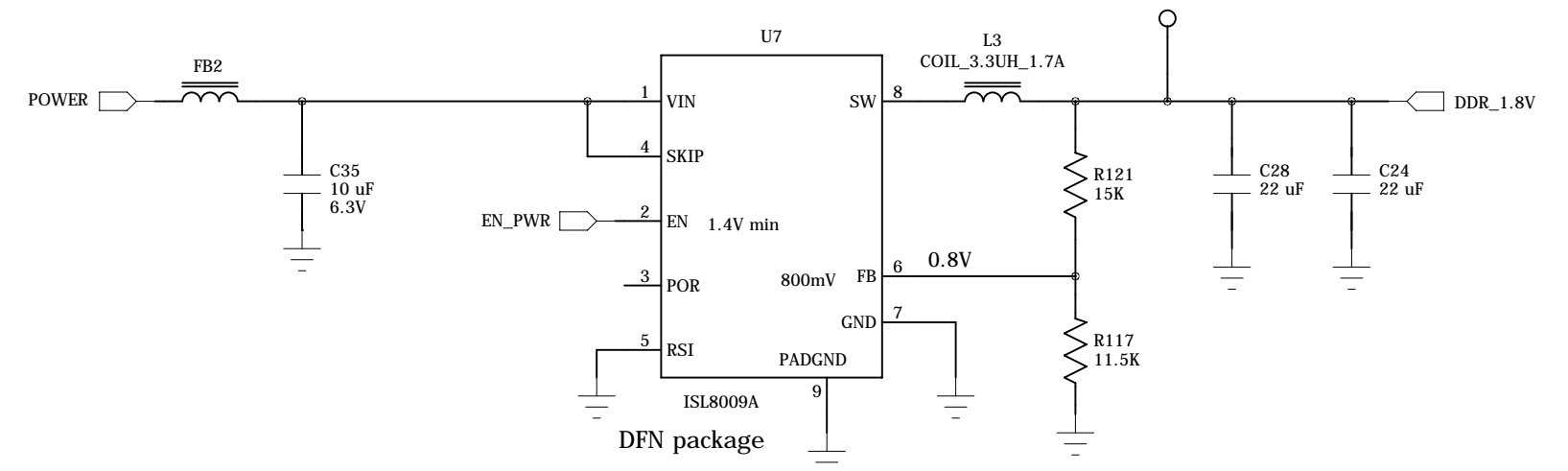
Power Sequence

3.3V rail comes up first

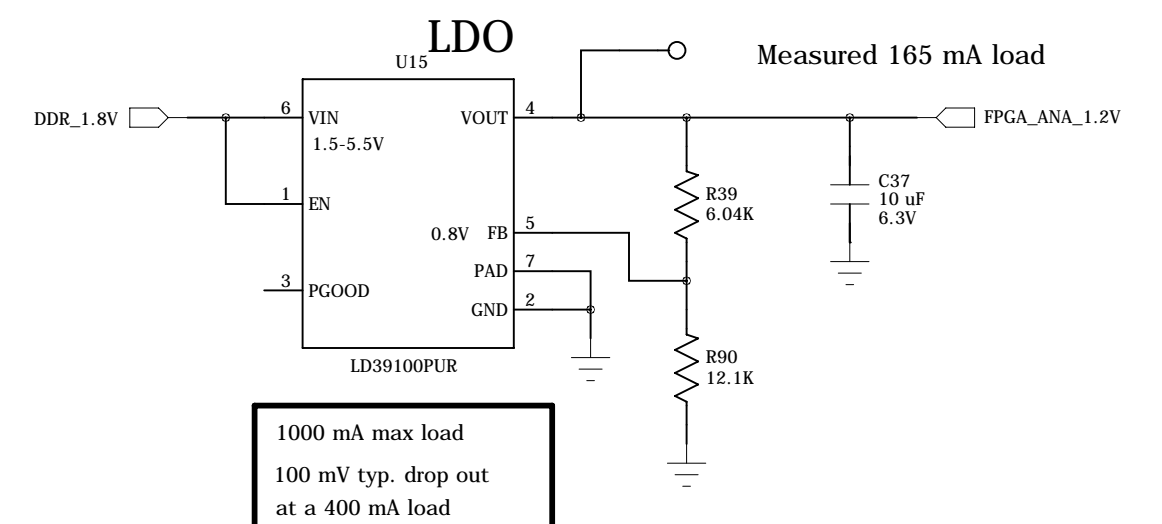
Then about 1 mS later

The Core_1.2V and the 1.8V rail come up together

1.8V DDR2 Power Supply

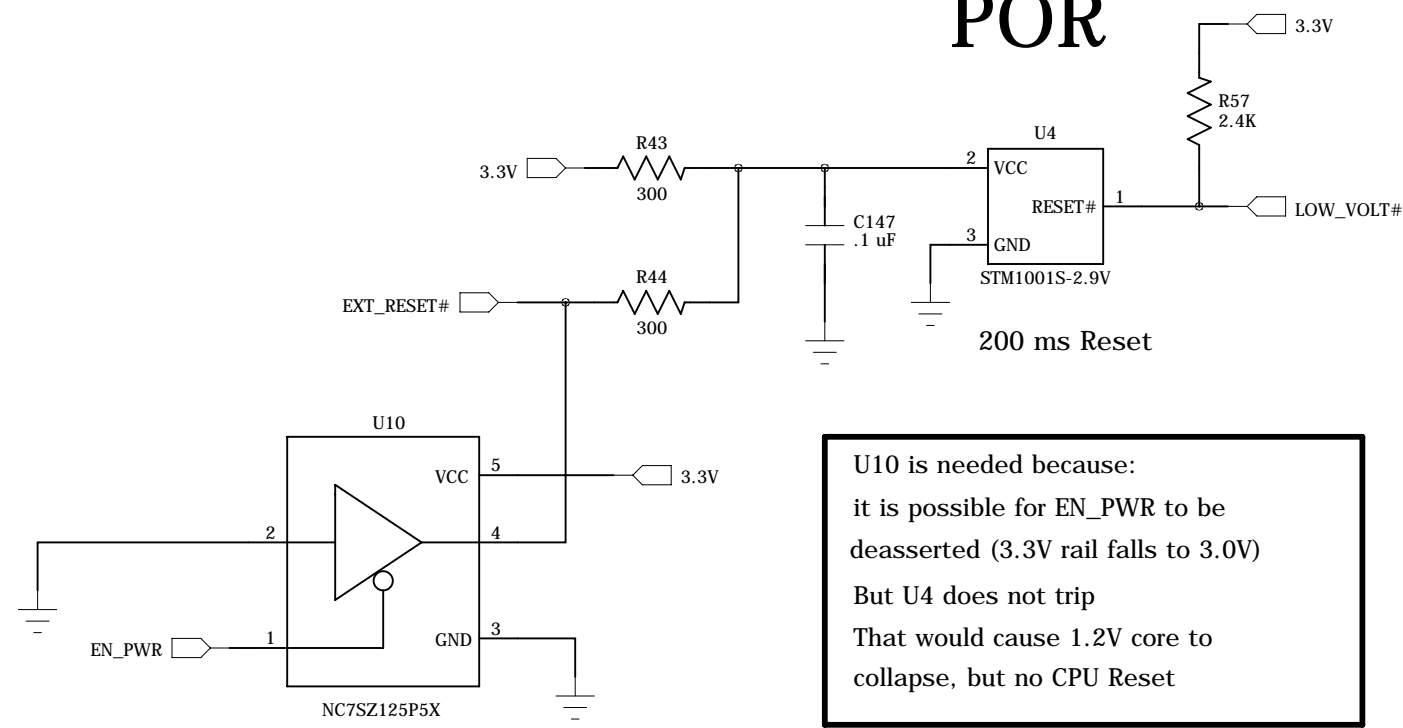


FPGA Analog 1.2V Reg.



1000 mA max load
100 mV typ. drop out at a 400 mA load

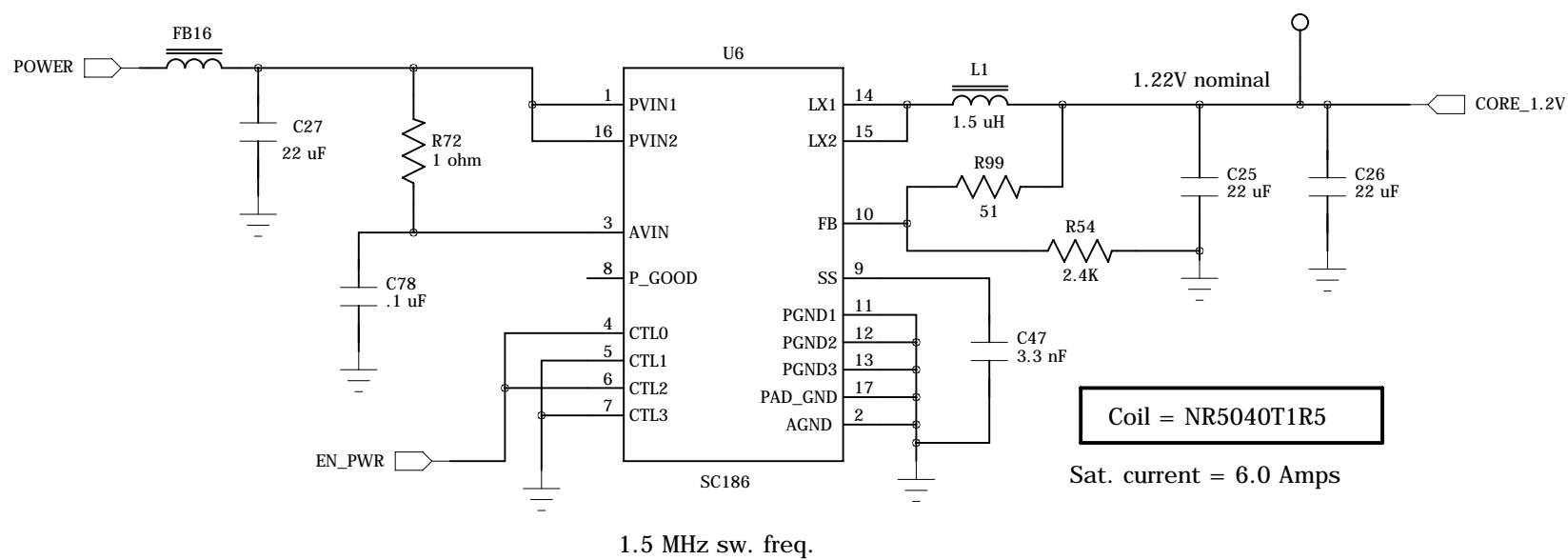
POR



U10 is needed because:
it is possible for EN_PWR to be deasserted (3.3V rail falls to 3.0V)
But U4 does not trip
That would cause 1.2V core to collapse, but no CPU Reset

1.2V Power Supply

up to 4000 mA

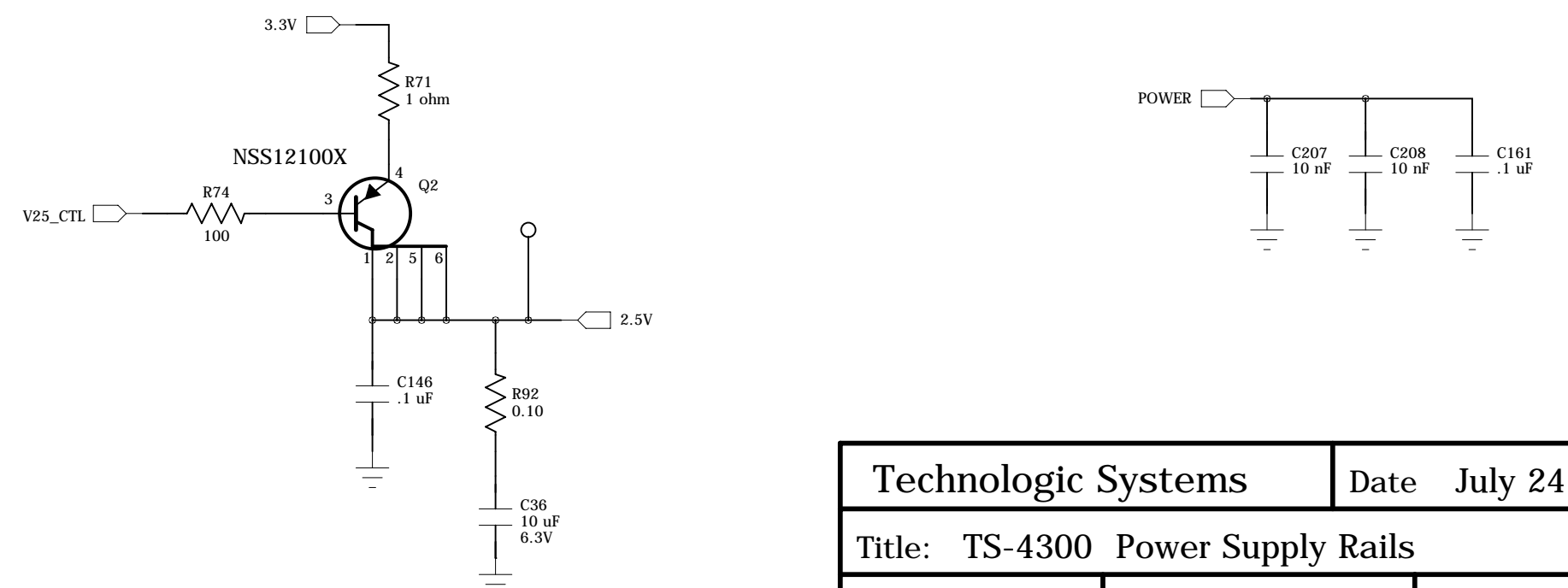


Coil = NR5040T1R5

Sat. current = 6.0 Amps

1.5 MHz sw. freq.

2.5V Power Supply

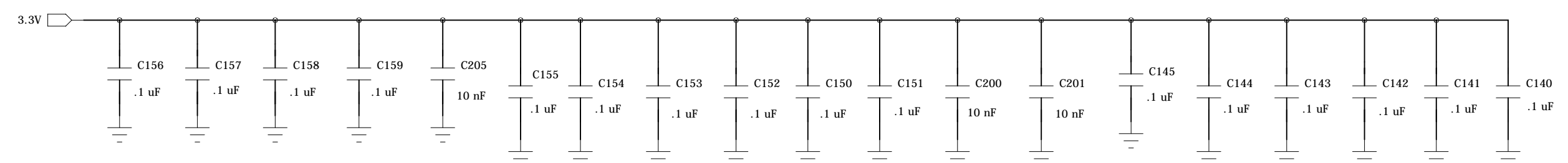
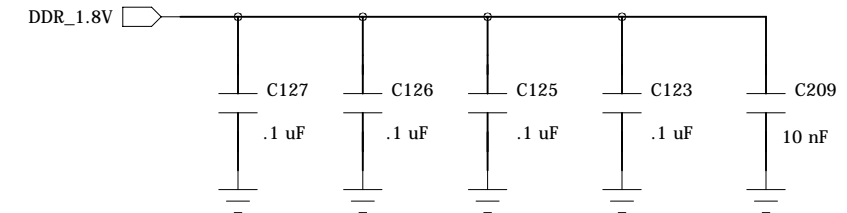
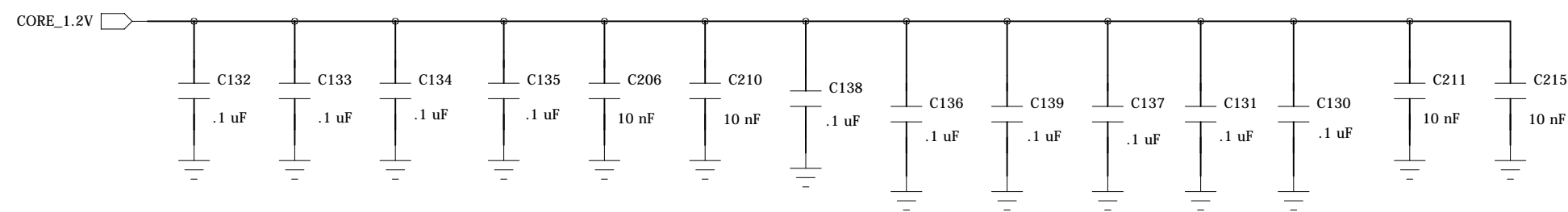
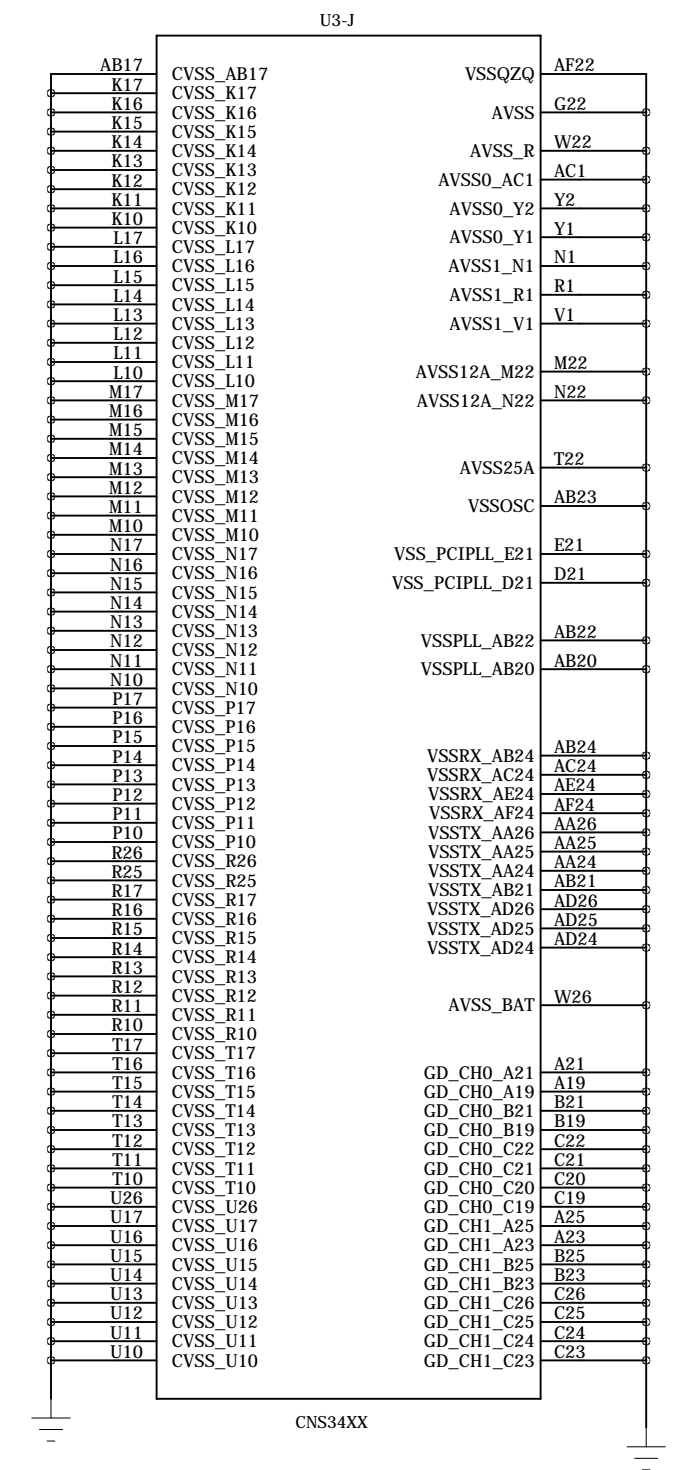
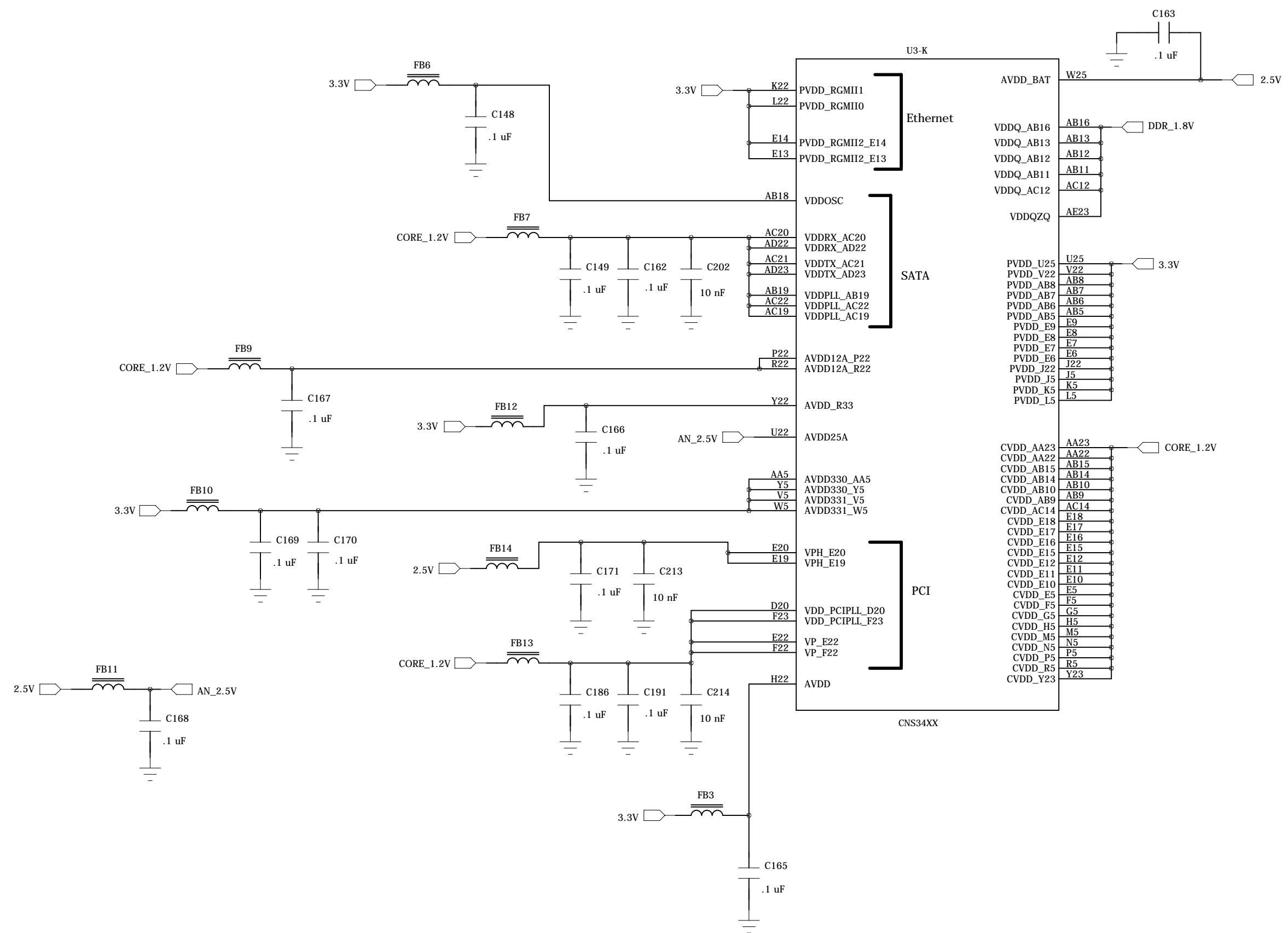


GND Test Point

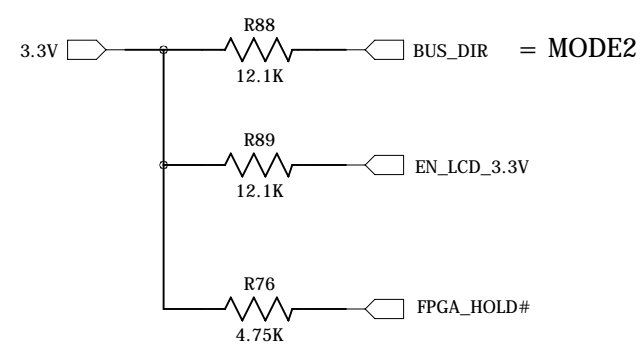
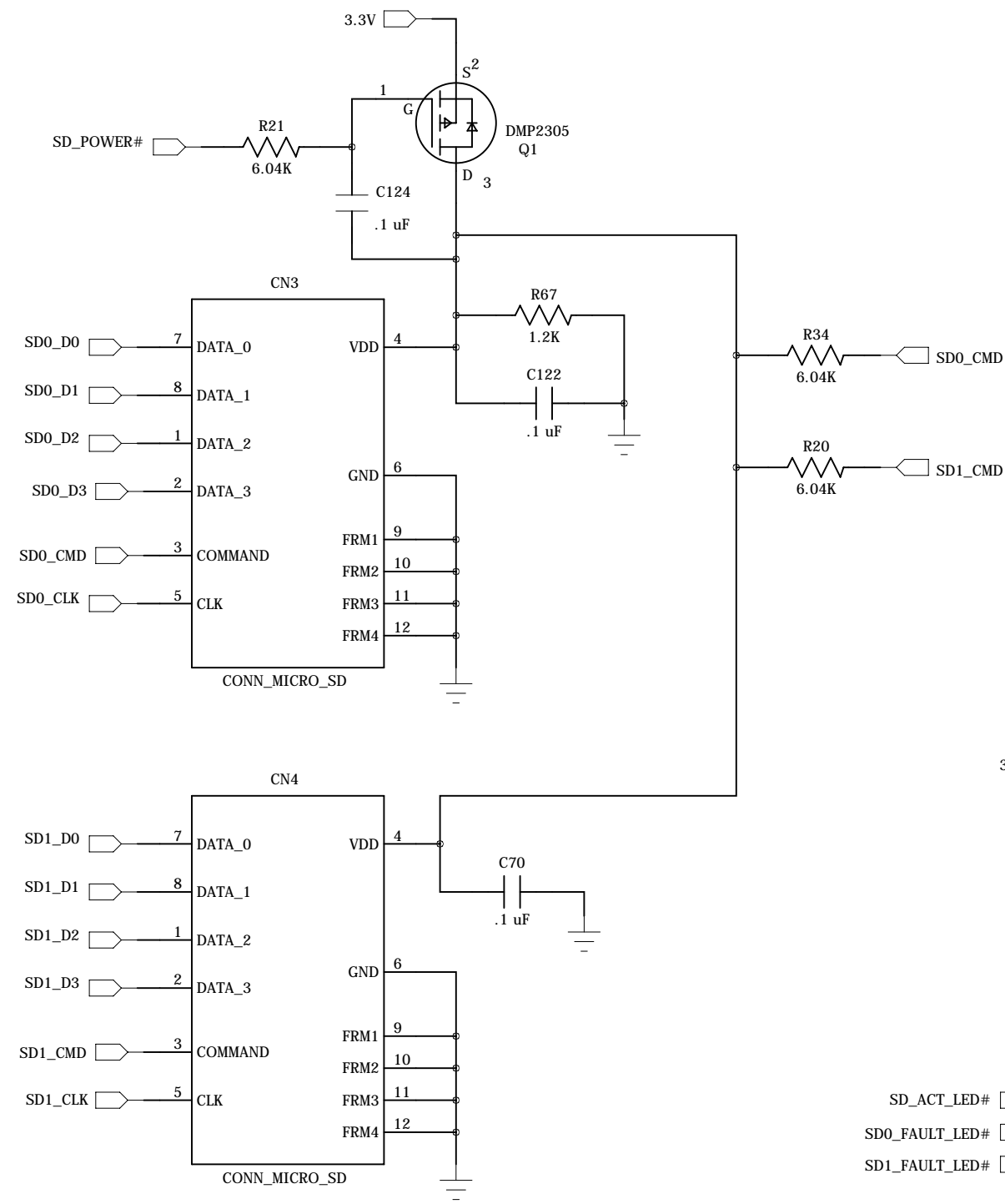


Technologic Systems	Date July 24, 2012
Title: TS-4300 Power Supply Rails	
Rev: B	Designer
Sheet 7 of 10	

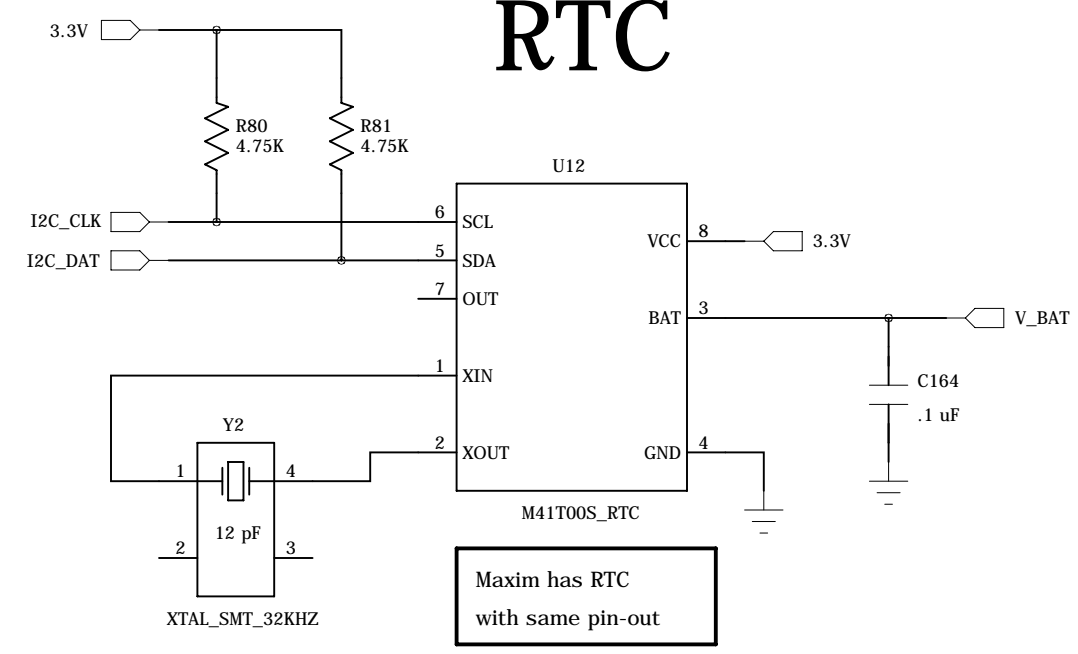
CPU Power



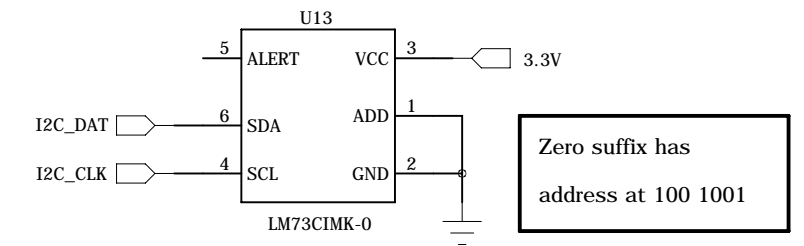
Micro SD Card Socket



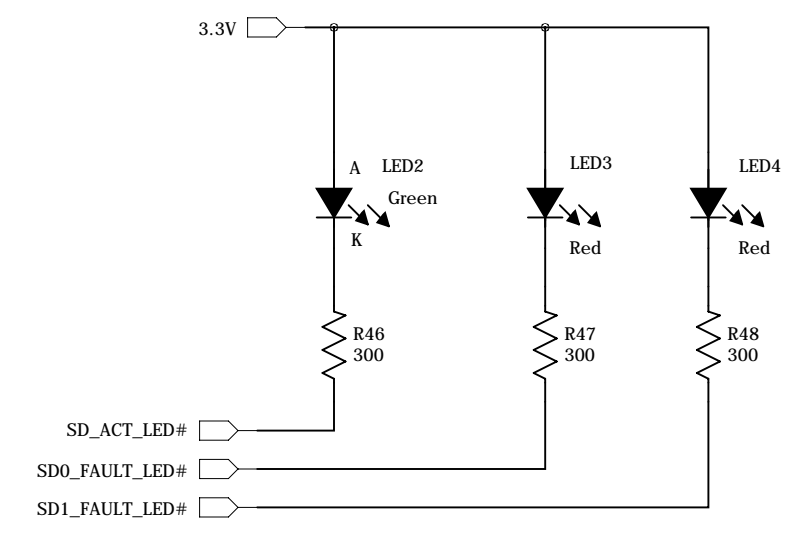
RTC



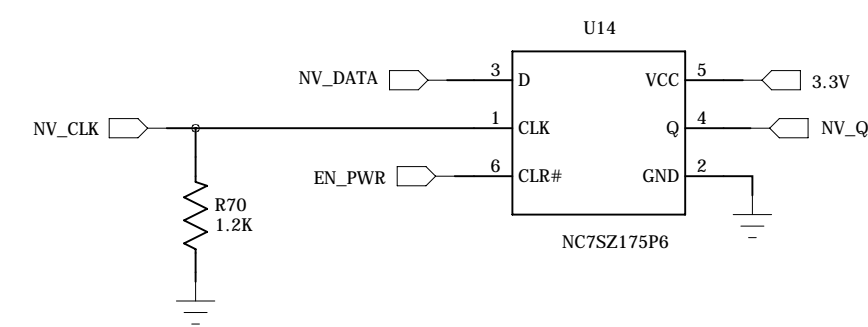
Temp Sensor



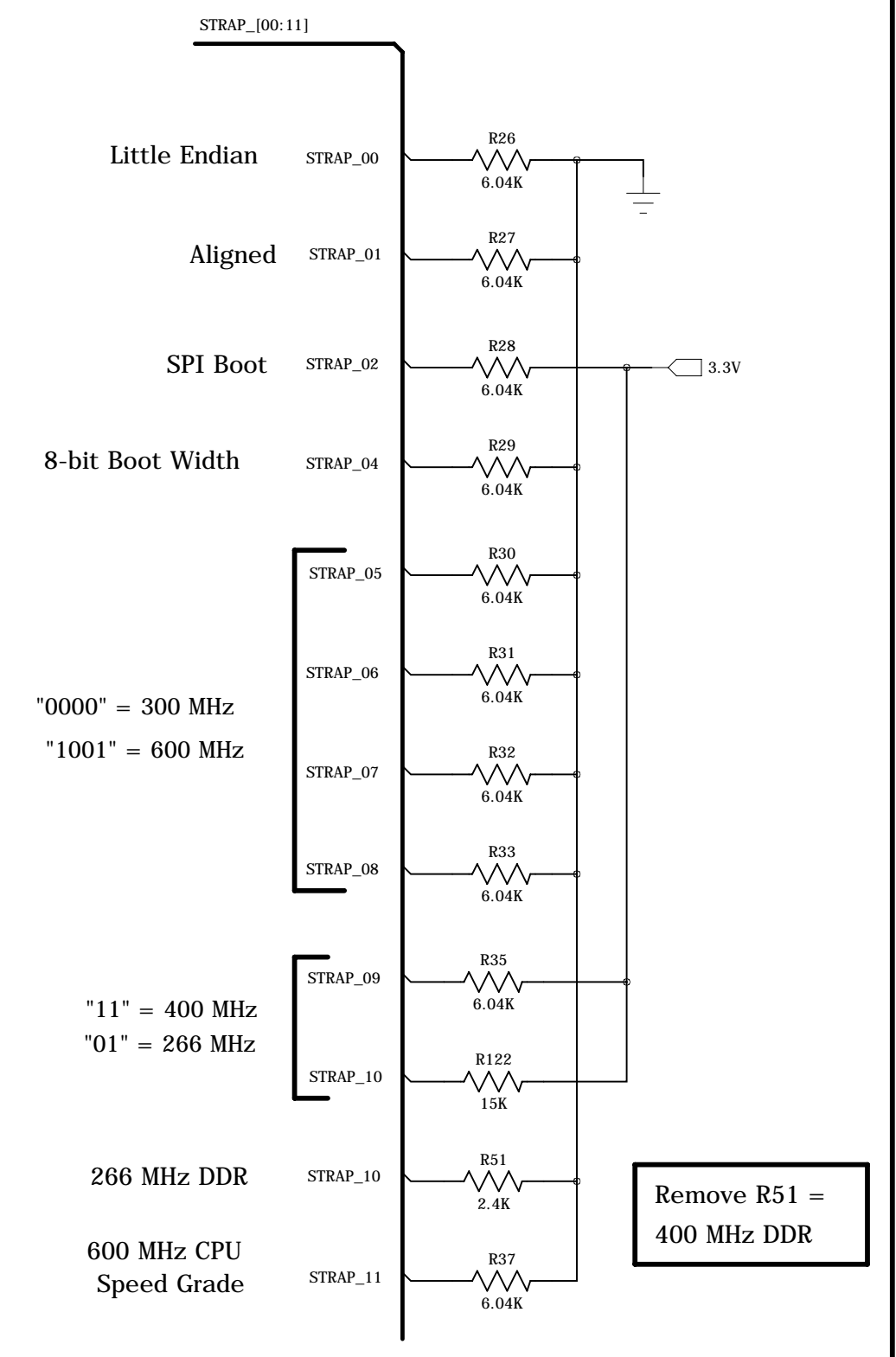
SD LEDs



Reboot Flag



Boot Strap Bias Resistors



Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.0V to 5.5V to these pins

OFF_BD_RESET# is an Output
used to reset all peripherals

EXT_RESET# is an Input
used to reboot the CPU

EXT_RESET# can
never be driven high
(use Open drain)

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

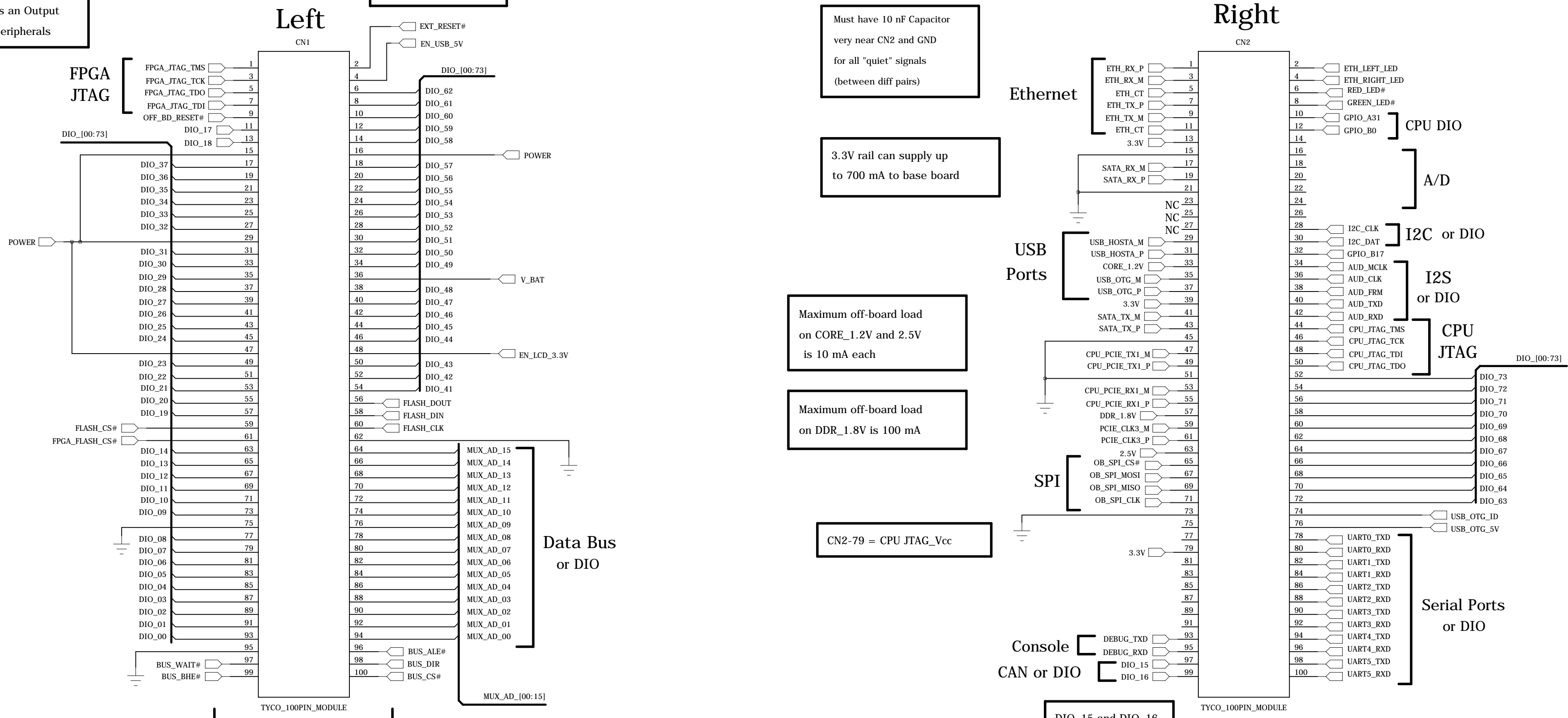
3.3V rail can supply up
to 700 mA to base board

Maximum off-board load
on CORE_1.2V and 2.5V
is 10 mA each

Maximum off-board load
on DDR_1.8V is 100 mA

CN2-79 = CPU JTAG_Vcc

DIO_15 and DIO_16
can be CAN_TXD
and CAN_RXD



Bus Control

Boot Strap

Mode 2	TS-4300 Boots from
1	SD Card
0	SD Card

BUS_DIR = MODE2

BUS_DIR is latched prior to
OFF_BD_RESET# deassertion

Connect 1.5K ohm resistor
between BUS_DIR and
OFF_BD_RESET# to set low
(Boot from SD card)

If Bus is not needed, all Bus
signals can be changed to DIO

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads