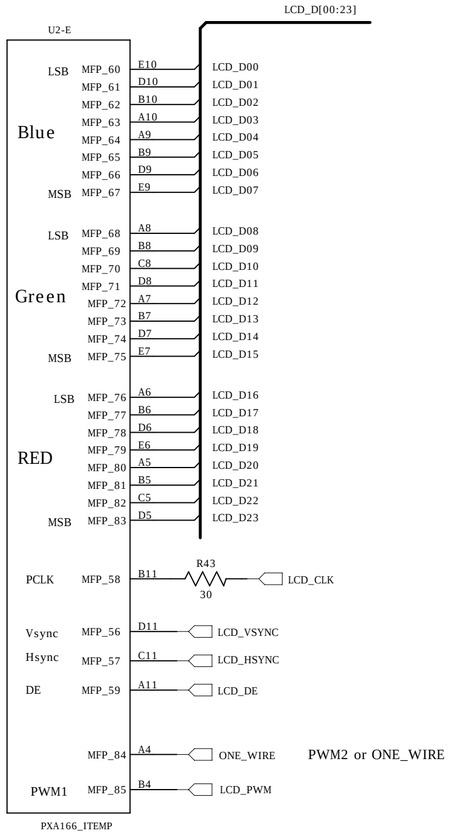
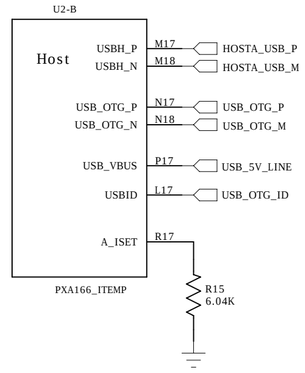
PXA166 800 MHz - PXA168 1066 MHz

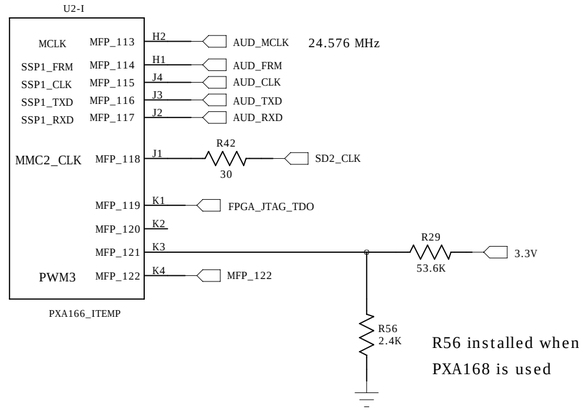
LCD



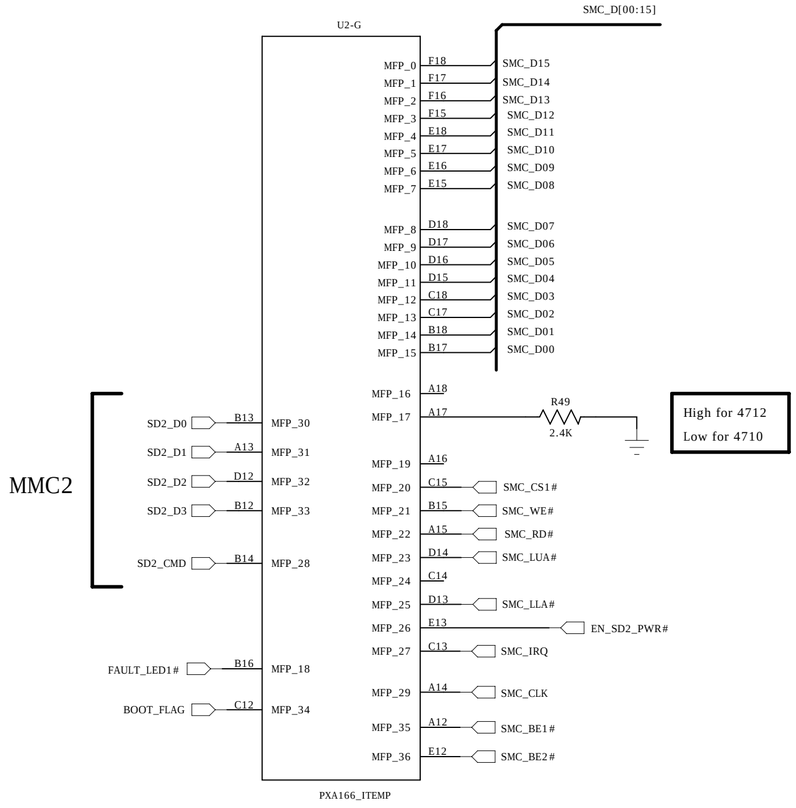
USB Ports



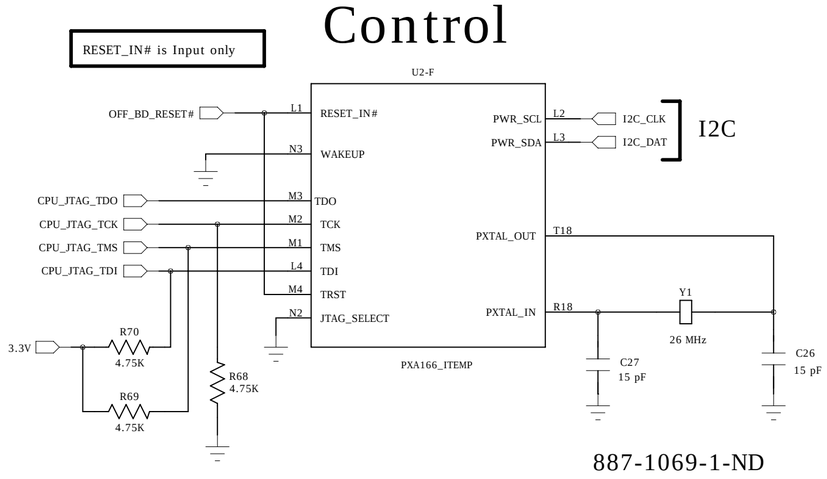
I2S



SMC Bus

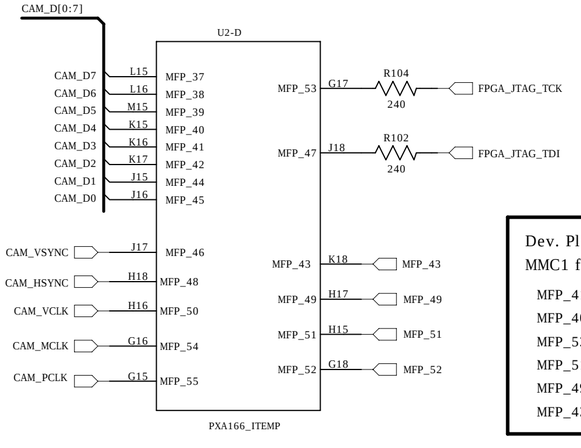


Control



887-1069-1-ND

Camera



Dev. Plat. uses
MMC1 for SD card

- MFP_41 = D0
- MFP_40 = D1
- MFP_52 = D2
- MFP_51 = D3
- MFP_49 = CMD
- MFP_43 = CLK

Technologic Systems	Date Jan. 3, 2013	
Title: TS-4710 Marvell PXA166 or PXA168		
Rev: A	Designer	Sheet 1 of 10

DDR3 x8 RAM

2 Gbit RAM chips

512 MB RAM Total

RAM_A[00:14]

CPU

U2-A

RAM_A00	R10	MA_0
RAM_A01	U10	MA_1
RAM_A02	V10	MA_2
RAM_A03	R11	MA_3
RAM_A04	U11	MA_4
RAM_A05	V11	MA_5
RAM_A06	V12	MA_6
RAM_A07	U12	MA_7
RAM_A08	T12	MA_8
RAM_A09	R12	MA_9
RAM_A10	V13	MA_10
RAM_A11	U13	MA_11
RAM_A12	R13	MA_12
RAM_A13	P13	MA_13
RAM_A14	R14	MA_14
RAM_BA0	T9	SDBA0
RAM_BA1	R9	SDBA1
RAM_BA2	P10	SDBA2
RAM_RAS#	V8	SDRAS#
RAM_CAS#	V9	SDCAS#
RAM_WE#	U9	SDWE#
RAM_CS0#	R8	SDCS0#
RAM_CKE0	R7	SDCKE0
RAM_CLK	V6	SDCLK0
RAM_CLK#	V7	SDCLK0#
RAM_LDM	P1	DQM0
RAM_UDM	V2	DQM1
RAM_LDQS	T1	DQS0
RAM_LDQS#	R1	DSQ0#
RAM_UDQS	V5	DSQS1
RAM_UDQS#	V4	DQS1#
RAM_ODT0	U8	ODT

RAM_D[00:15]

MDQ_0	P2	RAM_D04
MDQ_1	P3	RAM_D02
MDQ_2	P4	RAM_D00
MDQ_3	R3	RAM_D05
MDQ_4	T3	RAM_D06
MDQ_5	U1	RAM_D01
MDQ_6	U2	RAM_D03
MDQ_7	V1	RAM_D07
MDQ_8	V3	RAM_D12
MDQ_9	U4	RAM_D09
MDQ_10	R5	RAM_D10
MDQ_11	T5	RAM_D14
MDQ_12	P6	RAM_D08
MDQ_13	R6	RAM_D13
MDQ_14	T6	RAM_D11
MDQ_15	U7	RAM_D15

SDCKE1	N9	
SDCS1#	N10	
ODT1	U14	
DDRESET#	V14	RAM_RST#
CALPAD	N4	R108 240
VREF	N1	R66 4.75K, R76 4.75K, C188 .1 uF
SEC_CS_EN	N5	R24 6.04K

DDR_1.5V

Output

PXA166_ITEMP

3.3V

RAM_A[00:14]

U18

256MB

RAM_A00	K3	A0
RAM_A01	L7	A1
RAM_A02	L3	A2
RAM_A03	K2	A3
RAM_A04	L8	A4
RAM_A05	L2	A5
RAM_A06	M8	A6
RAM_A07	M2	A7
RAM_A08	N8	A8
RAM_A09	M3	A9
RAM_A10	H7	A10
RAM_A11	M7	A11
RAM_A12	K7	A12
RAM_A13	N3	A13
RAM_A14	N7	A14
	A3	NC
	F1	NC
	F9	NC
	H1	NC
	H9	NC
	J7	NC
	A7	NU
RAM_RST#	N2	RESET#
RAM_BA0	J2	BA0
RAM_BA1	K8	BA1
RAM_BA2	J3	BA2
RAM_CLK	F7	CK
RAM_CLK#	G7	CK#
RAM_CKE0	G9	CKE
RAM_CS0#	H2	CS#
RAM_RAS#	F3	RAS#
RAM_CAS#	G3	CAS#
RAM_WE#	H3	WE#
RAM_ODT0	G1	ODT
RAM_VREF	E1	VREF
	J8	VREF

VDD0	A2	DDR_1.5V
VDD1	A9	
VDD2	D7	
VDD3	G2	
VDD4	G8	
VDD5	K1	
VDD6	K9	
VDD7	M1	
VDD8	M9	
VDDQ0	B9	
VDDQ1	C1	
VDDQ2	E2	
VDDQ3	E9	

RAM_D[00:15]

DQ0	B3	RAM_D00
DQ1	C7	RAM_D01
DQ2	C2	RAM_D02
DQ3	C8	RAM_D03
DQ4	E3	RAM_D04
DQ5	E8	RAM_D05
DQ6	D2	RAM_D06
DQ7	E7	RAM_D07
DQS	C3	RAM_LDQS
DQS#	D3	RAM_LDQS#
DM	B7	RAM_LDM
ZQ	H8	R105 240
VSSQ0	B2	
VSSQ1	B8	
VSSQ2	C9	
VSSQ3	D1	
VSSQ4	D9	

VSS0	A1	
VSS1	A8	
VSS2	B1	
VSS3	D8	
VSS4	F2	
VSS5	F8	
VSS6	J1	
VSS7	J9	
VSS8	L1	
VSS9	L9	
VSS10	N1	
VSS11	N9	

RAM_DDR3_X8_78BALL

C196 .1 uF, C197 .1 uF

RAM_A[00:14]

U20

256MB

RAM_A00	K3	A0
RAM_A01	L7	A1
RAM_A02	L3	A2
RAM_A03	K2	A3
RAM_A04	L8	A4
RAM_A05	L2	A5
RAM_A06	M8	A6
RAM_A07	M2	A7
RAM_A08	N8	A8
RAM_A09	M3	A9
RAM_A10	H7	A10
RAM_A11	M7	A11
RAM_A12	K7	A12
RAM_A13	N3	A13
RAM_A14	N7	A14
	A3	NC
	F1	NC
	F9	NC
	H1	NC
	H9	NC
	J7	NC
	A7	NU
RAM_RST#	N2	RESET#
RAM_BA0	J2	BA0
RAM_BA1	K8	BA1
RAM_BA2	J3	BA2
RAM_CLK	F7	CK
RAM_CLK#	G7	CK#
RAM_CKE0	G9	CKE
RAM_CS0#	H2	CS#
RAM_RAS#	F3	RAS#
RAM_CAS#	G3	CAS#
RAM_WE#	H3	WE#
RAM_ODT0	G1	ODT
RAM_VREF	E1	VREF
	J8	VREF

VDD0	A2	DDR_1.5V
VDD1	A9	
VDD2	D7	
VDD3	G2	
VDD4	G8	
VDD5	K1	
VDD6	K9	
VDD7	M1	
VDD8	M9	
VDDQ0	B9	
VDDQ1	C1	
VDDQ2	E2	
VDDQ3	E9	

RAM_D[00:15]

DQ0	B3	RAM_D08
DQ1	C7	RAM_D09
DQ2	C2	RAM_D10
DQ3	C8	RAM_D11
DQ4	E3	RAM_D12
DQ5	E8	RAM_D13
DQ6	D2	RAM_D14
DQ7	E7	RAM_D15
DQS	C3	RAM_UDQS
DQS#	D3	RAM_UDQS#
DM	B7	RAM_UDM
ZQ	H8	R103 240
VSSQ0	B2	
VSSQ1	B8	
VSSQ2	C9	
VSSQ3	D1	
VSSQ4	D9	

VSS0	A1	
VSS1	A8	
VSS2	B1	
VSS3	D8	
VSS4	F2	
VSS5	F8	
VSS6	J1	
VSS7	J9	
VSS8	L1	
VSS9	L9	
VSS10	N1	
VSS11	N9	

RAM_DDR3_X8_78BALL

C175 .1 uF, C117 .1 uF

RAM_UDQS#, RAM_LDQS# — R82 1.2K, R83 1.2K — DDR_1.5V

RAM_UDQS, RAM_LDQS — R84 1.2K, R85 1.2K

RAM_CKE0 — R67 4.75K

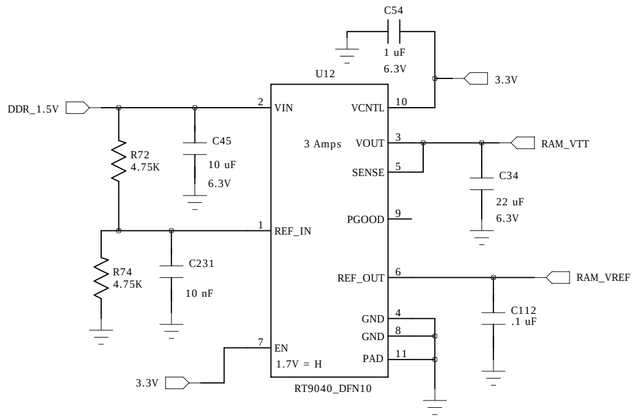
RAM_CLK — R94 51, R99 51, C236 10 nF — RAM_CLK#

C111 .1 uF, C174 .1 uF, C173 .1 uF, C172 .1 uF, C166 .1 uF, C110 .1 uF, C177 .1 uF, C178 .1 uF — DDR_1.5V

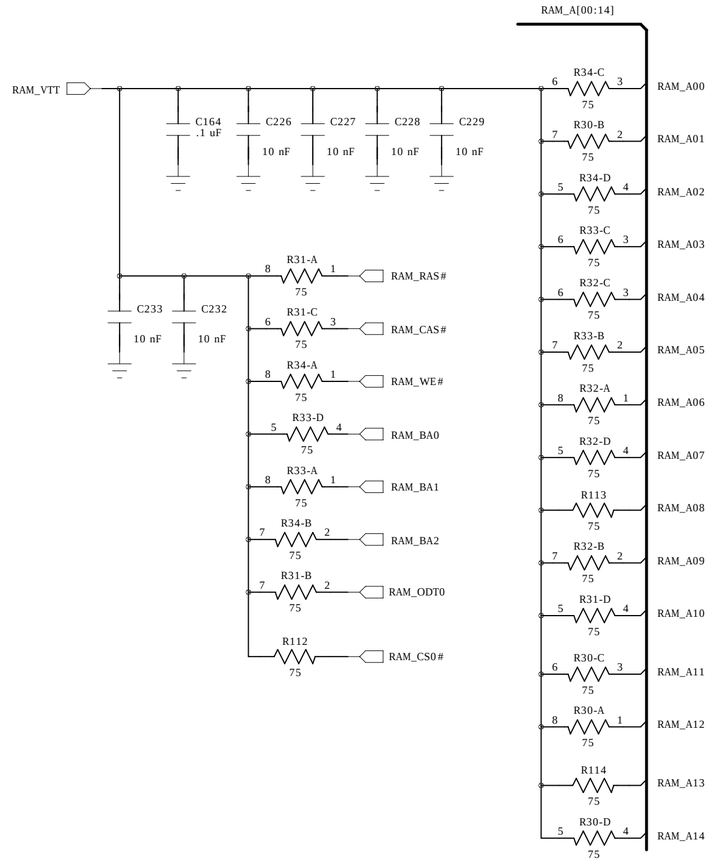
C186 .1 uF, C179 .1 uF, C180 .1 uF, C181 .1 uF — DDR_1.5V

Technologic Systems	Date Jan. 3, 2013	
Title: TS-4710 DDR3 RAM		
Rev: A	Designer	Sheet 2 of 10

DDR3 RAM Termination Power Supply



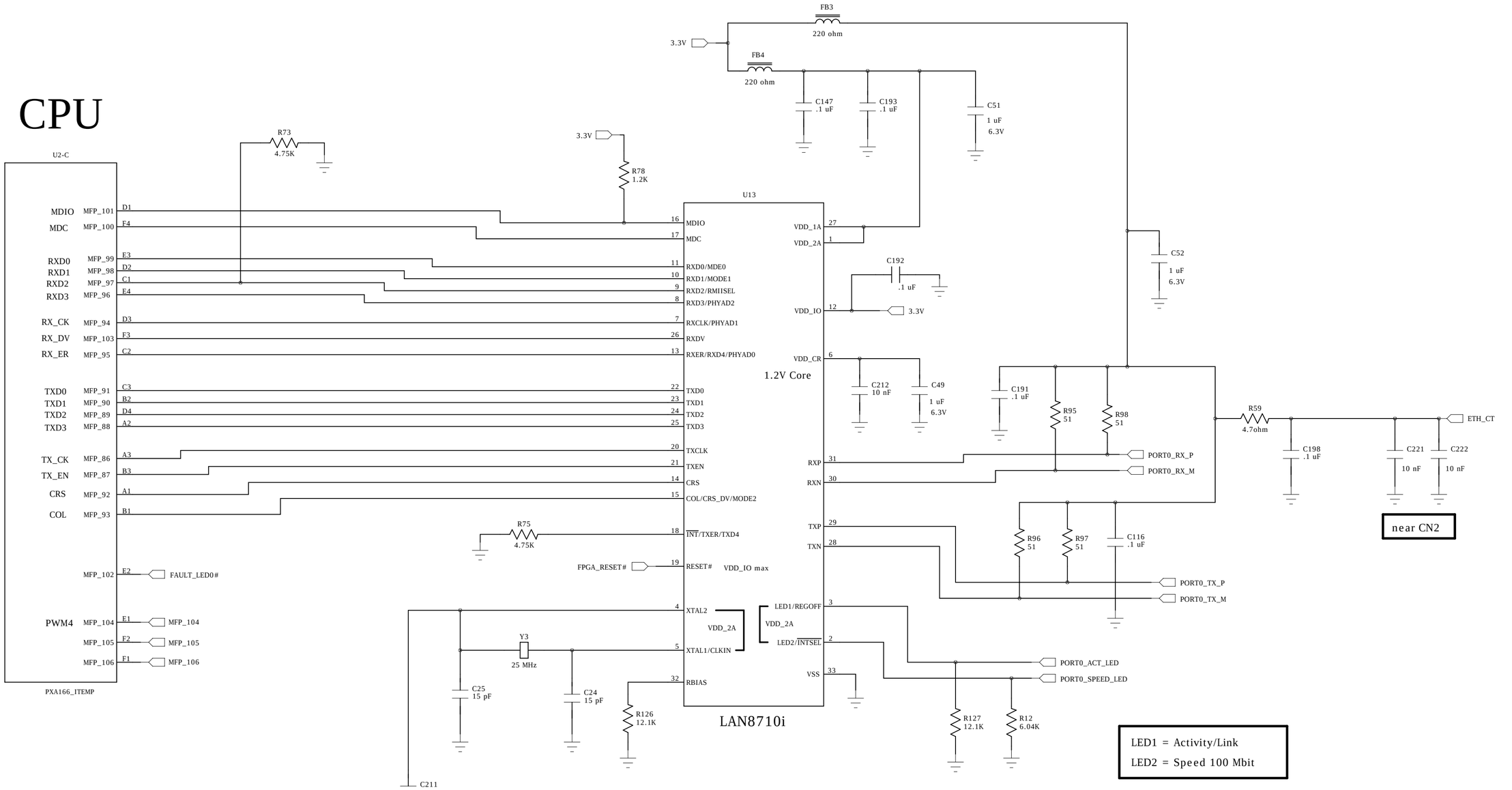
Termination Resistors



Technologic Systems		Date Jan. 3, 2013
Title: TS-4710 DDR3 RAM		
Rev: A	Designer	Sheet 3 of 10

10/100 Ethernet

CPU



Technologic Systems	Date Jan. 3, 2013	
Title: TS-4710 Ethernet		
Rev: A	Designer RLM	Sheet 4 of 10

FPGA with 5K or 8K LUTs

SMC Bus from CPU

Off Bd. LEDs

XUARTs

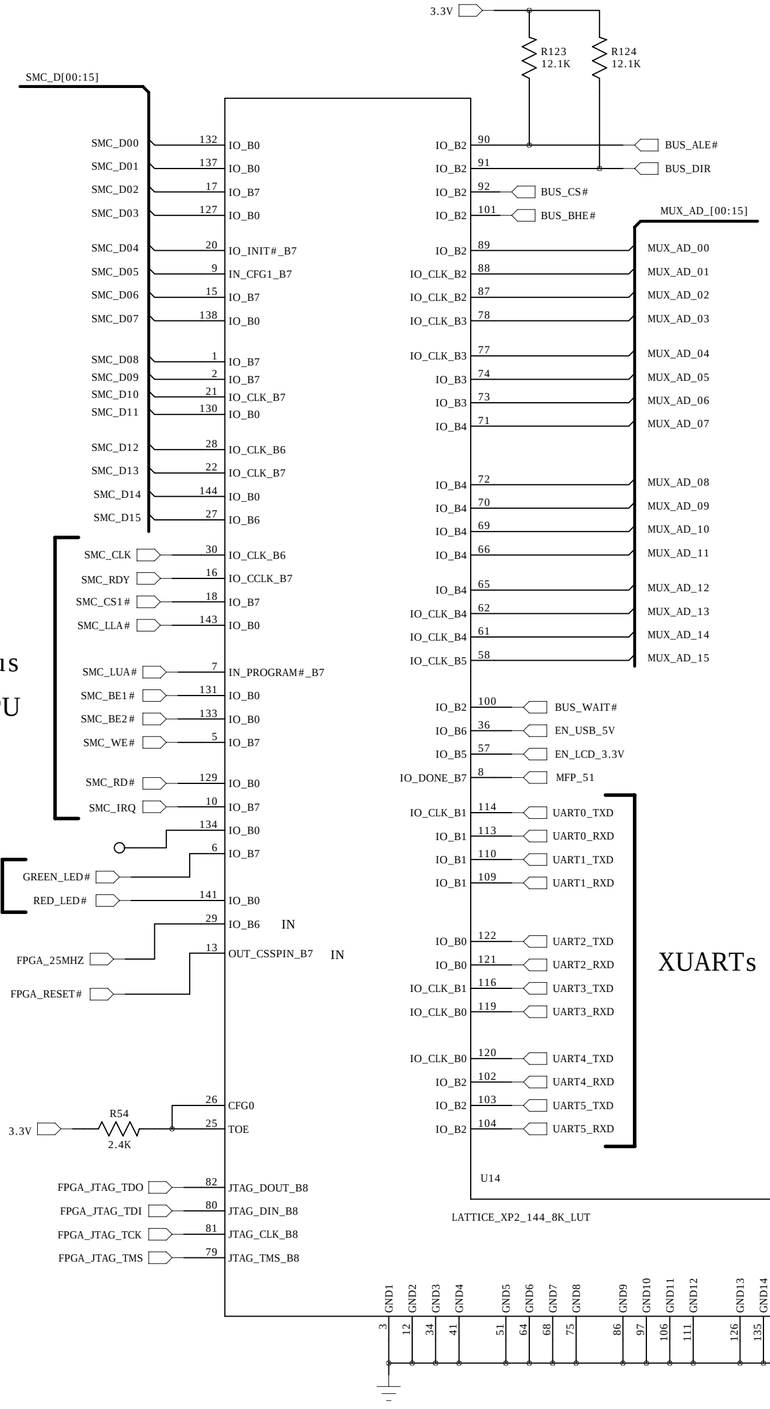
SD Cards

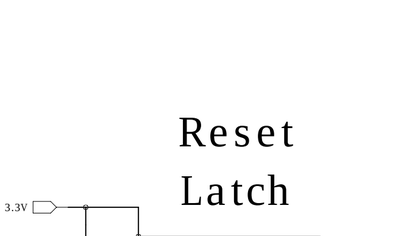
SPI Bus

CPU USB Power

Reset Latch

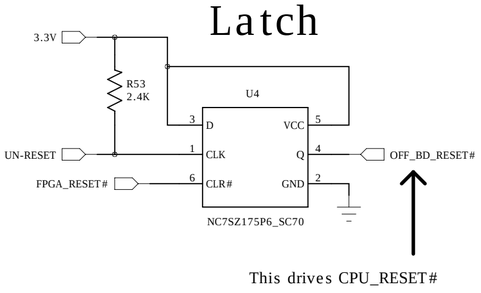
FPGA 1.2V Reg.



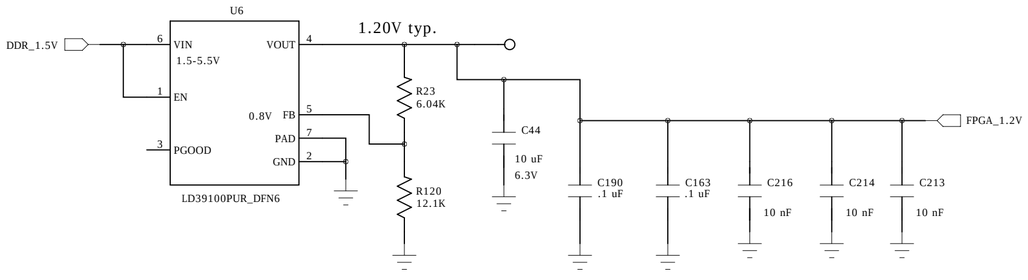


XP2-5 has:
5K or 8K LUTS 2 PLLs
9/12 blocks of 1Kx18 Block RAM
12 18x18 Multipliers

100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min



This drives CPU_RESET#

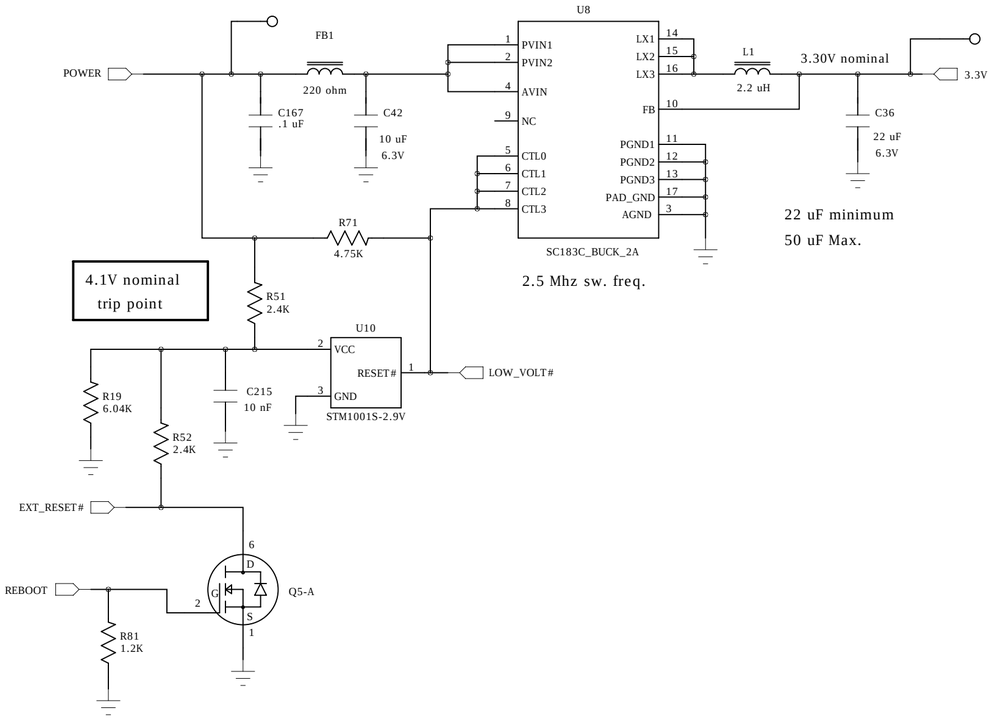


Technologic Systems		Date Jan. 3, 2013
Title: TS-4710 FPGA		
Rev: A	Designer	Sheet 5 of 10

Power Supplies

#1 3.3V Power Supply

up to 2000 mA



Power Supply Sequence:

When POWER < 4.1V all rails OFF

After POWER is > 4.1V
Then wait 200 mS

#1 Turn on 3.3V Rail

#2 AVDD (1.8V) is always
slightly lower than 3.3V rail
Then wait 1 mS, and enable

#3 CPU Core rail
Wait 4 ms
then enable:

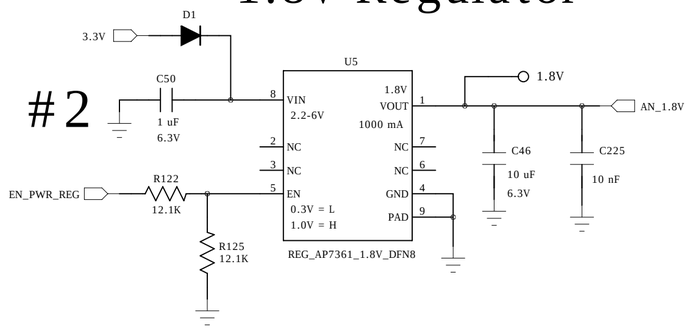
#4 DDR 1.5V Rail

#5 FPGA 1.2V ramps simultaneous
with DDR_1.5V rail

#6 FPGA controls delay until
AVDD_OTG rail is enabled

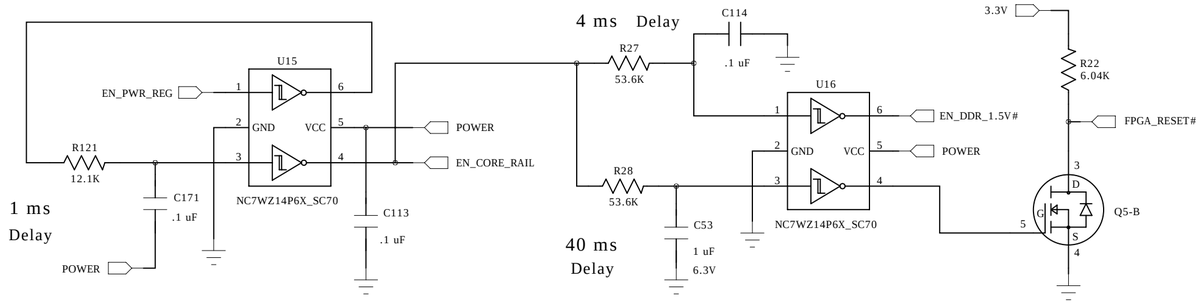
All Power rails are turned off
at the same time (within 5 ms)

Analog
1.8V Regulator

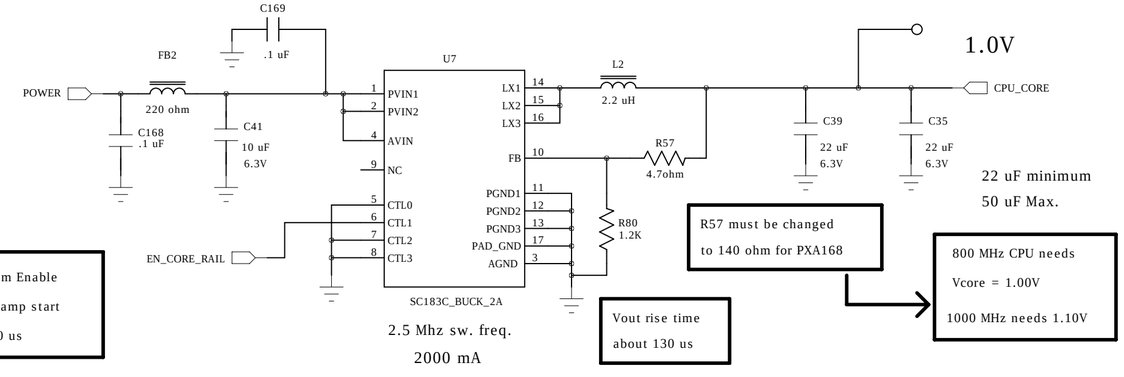


GND

Power Sequencer



#3 CPU Core Supply



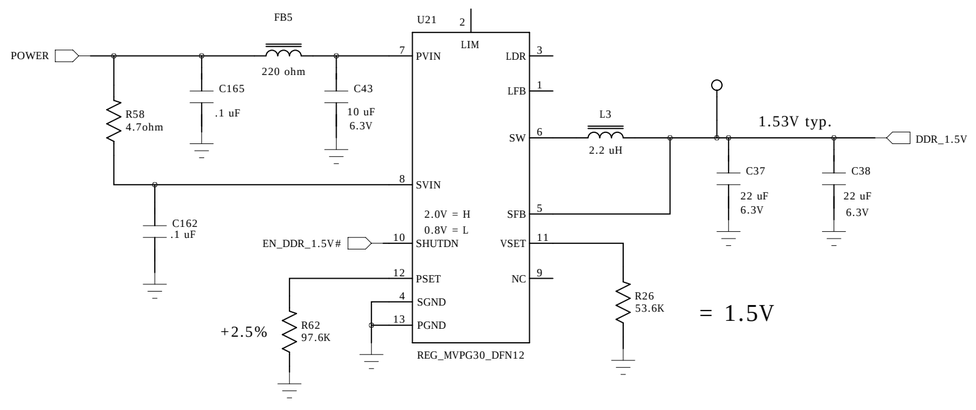
Delay from Enable
to Vout ramp start
is typ. 50 us

R57 must be changed
to 140 ohm for PXA168

800 MHz CPU needs
Vcore = 1.00V
1000 MHz needs 1.10V

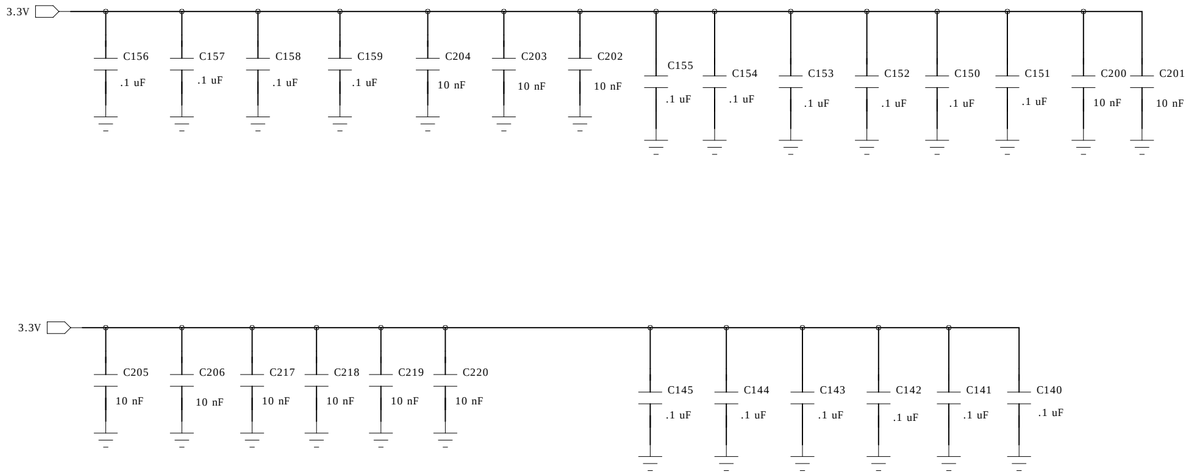
Vout rise time
about 130 us

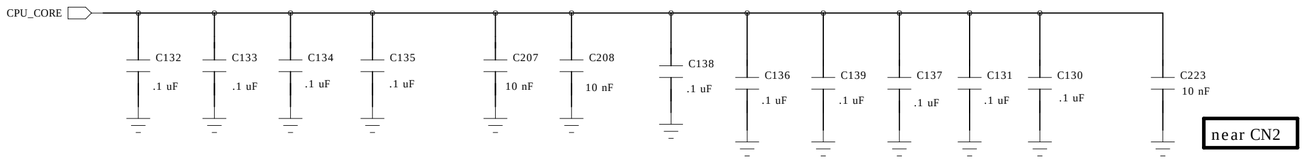
#4 DDR3 1.5V Reg.

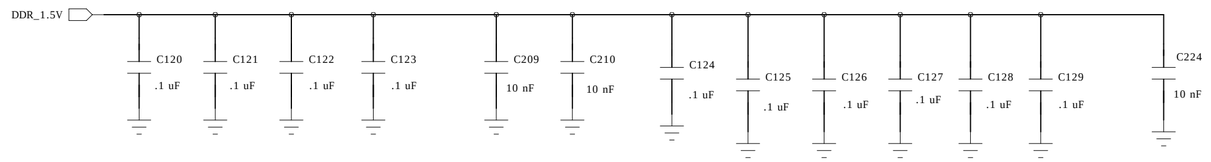


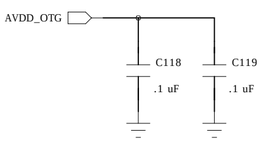
Technologic Systems	Date Jan. 3, 2013	
Title: TS-4710 Power Supplies		
Rev: A	Designer	Sheet 6 of 10

CPU Power



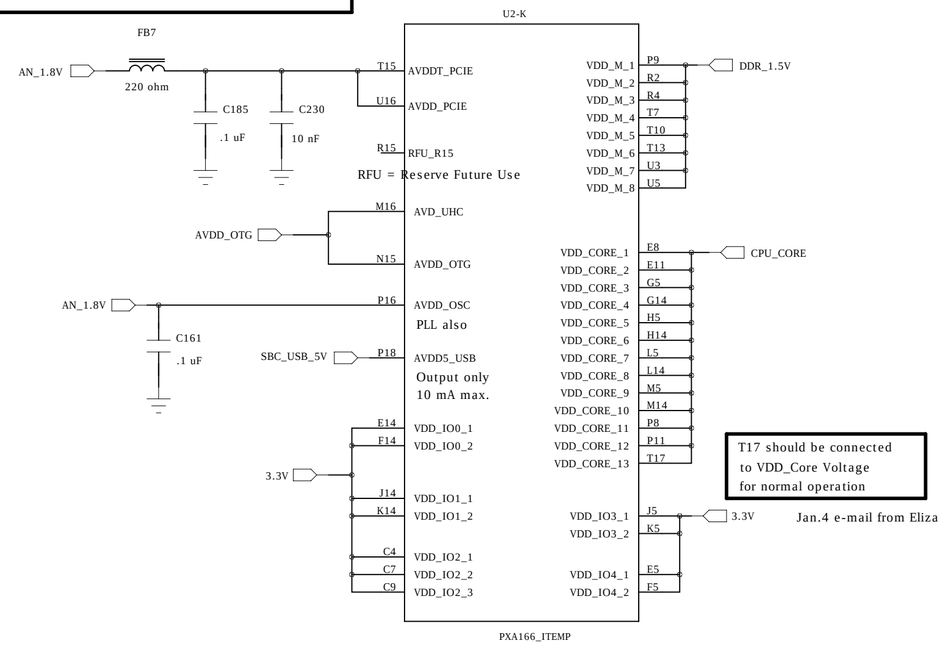




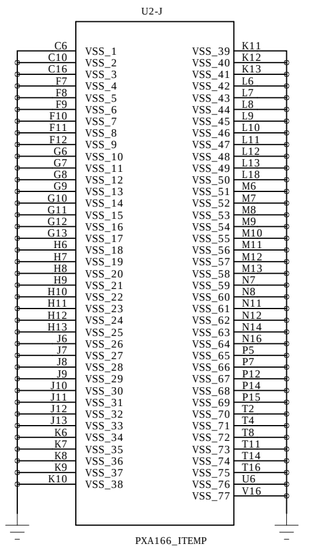


PXA168 PCIE rails must be connected to AVDD_OSC (1.8V)

CPU



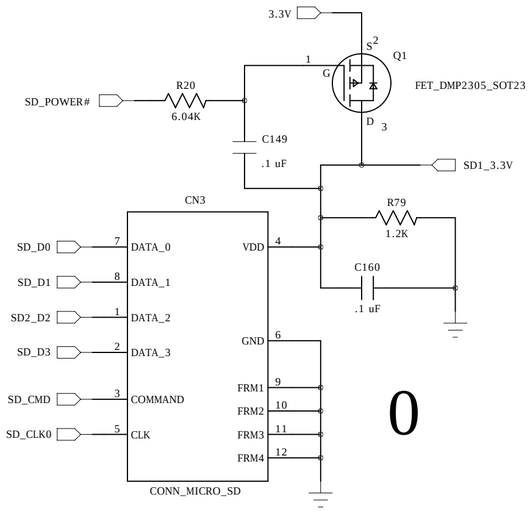
CPU



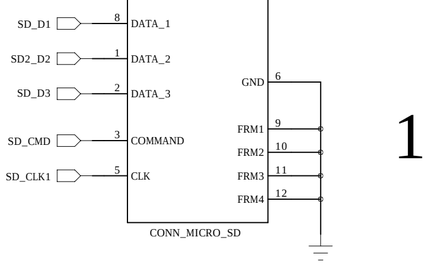
Technologic Systems	Date Jan. 3, 2013	
Title: TS-4710 CPU Power and Bypass caps		
Rev: A	Designer	Sheet 7 of 10

Jan.4 e-mail from Eliza

Micro SD Card Sockets

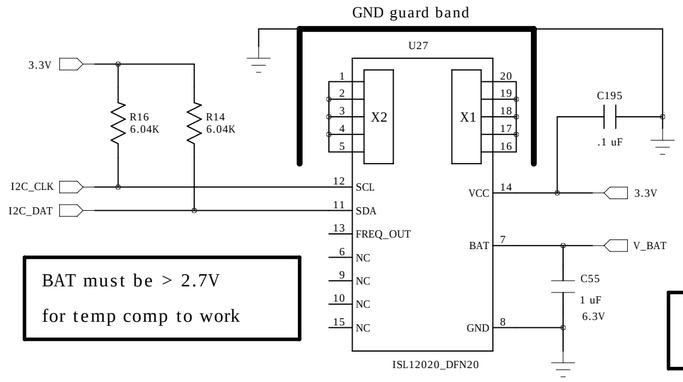


0



1

RTC and Temp. Sensor

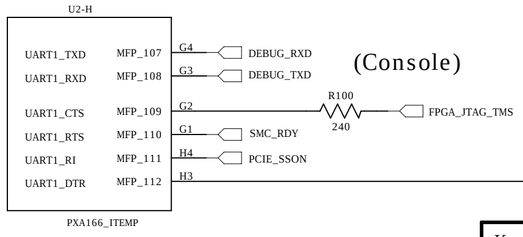


BAT must be > 2.7V
for temp comp to work

Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

CPU

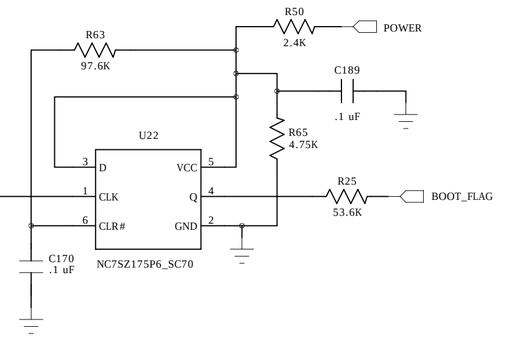
Debug UART



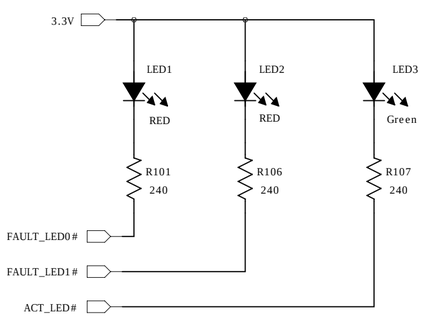
(Console)

Keep normally
at logic zero

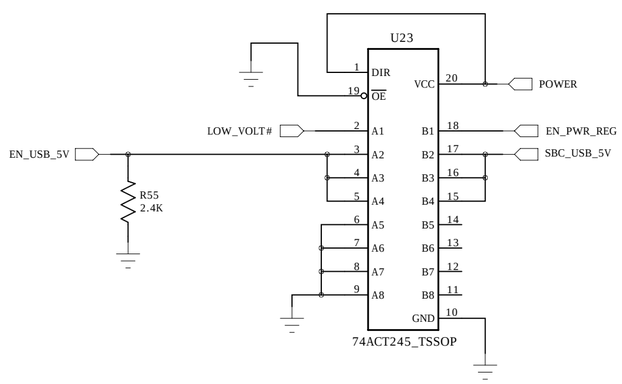
Reboot Flag



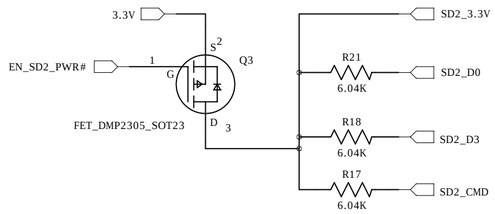
SD Card LEDs



3.3V --> 5V Level Shifter

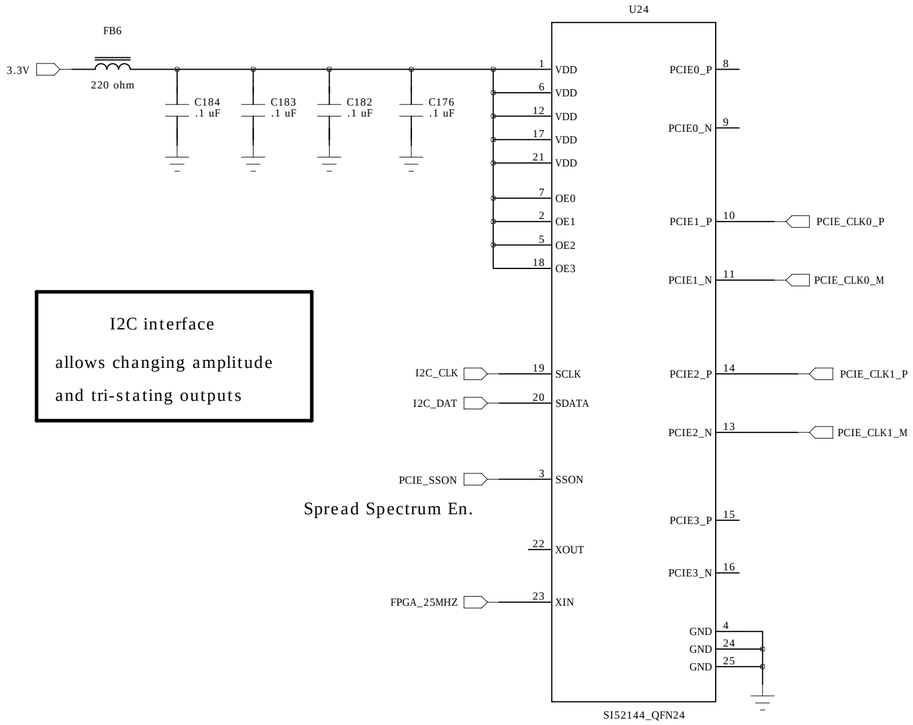


OFF BD. SD Card Power



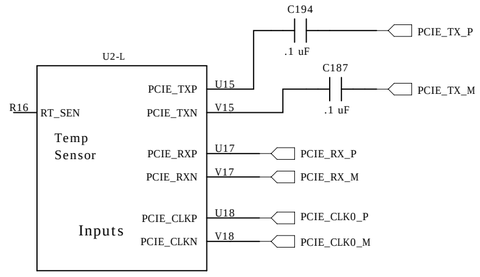
Technologic Systems	Date Jan. 3, 2013	
Title: TS-4710 SD card, RTC, Temp.		
Rev: A	Designer	Sheet 8 of 10

PCIe 100 MHz Clock Generator



CPU PCIe

PCIe not supported on PXA166



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Title: TS-4710 PCIe Clock and CPU PCIe		
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Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 400 mA

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

Left

CN1

FPGA JTAG
- FPGA_JTAG_TMS 1
- FPGA_JTAG_TCK 3
- FPGA_JTAG_TDO 5
- FPGA_JTAG_TDI 7
- OFF_BD_RESET# 9

OFF_BD_RESET# is an Output
used to reset all peripherals

NC 11
NC 13
POWER 15
POWER_FAIL# NC 17
LCD_D08 19
LCD_D09 21
LCD_D10 23
LCD_D11 25
LCD_D12 27
29
LCD_D13 31
LCD_D14 33
LCD_D15 35
LCD_D16 37
LCD_D17 39
LCD_D18 41
LCD_D19 43
LCD_D20 45
POWER 47
LCD_CLK 49
LCD_HSYNC 51
LCD_VSYNC 53
LCD_DE 55
LCD_PWM 57
59
61
DIO_14 63
DIO_13 65
DIO_12 67
DIO_11 69
DIO_10 71
DIO_09 73
75
DIO_08 77
DIO_07 79
DIO_06 81
DIO_05 83
DIO_04 85
DIO_03 87
DIO_02 89
DIO_01 91
DIO_00 93
95
BUS_WAIT# 97
BUS_BHE# 99

POWER
C146 .1 uF
C148 .1 uF

2 EXT_RESET#
4 EN_USB_5V
6 SD2_D2
8 SD2_D3
10 SD2_CMD
12 SD2_3.3V
14 SD2_CLK
16 POWER
18 SD2_D0
20 SD2_D1
22
24 LCD_D00
26 LCD_D01
28 LCD_D02
30 LCD_D03
32 LCD_D04
34 LCD_D05
36 V_BAT
38 LCD_D06
40 LCD_D07
42 LCD_D21
44 LCD_D22
46 LCD_D23
48 EN_LCD_3.3V
50
52
54
56
58
60
62
64 MUX_AD_15
66 MUX_AD_14
68 MUX_AD_13
70 MUX_AD_12
72 MUX_AD_11
74 MUX_AD_10
76 MUX_AD_09
78 MUX_AD_08
80 MUX_AD_07
82 MUX_AD_06
84 MUX_AD_05
86 MUX_AD_04
88 MUX_AD_03
90 MUX_AD_02
92 MUX_AD_01
94 MUX_AD_00
96 BUS_ALE#
98 BUS_DIR
100 BUS_CS#

Off-Bd SD Card
uses CPU MMC2

DIO_[00:16]
FPGA DIO
Data Bus or DIO
MUX_AD_[00:15]

TYCO_100PIN_MODULE

Bus Control

If Bus is not needed, all Bus signals can be changed to DIO

Devices connected to this bus must never drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

The data bus can not have more than 30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

Must have 10 nF Capacitor
very near CN2 and GND
for all "quiet" signals
(between diff pairs)

3.3V rail can supply up to 700 mA to base board

Maximum off-board load on AVDD_OSC is 10 mA

Right

CN2

Ethernet
- PORT0_RX_P 1
- PORT0_RX_M 3
- ETH_CT 5
- PORT0_TX_P 7
- PORT0_TX_M 9
- ETH_CT 11
- 3.3V 13
15
17
19
21
NC 23
NC 25
NC 27
29

USB Ports
- HOSTA_USB_M 31
- HOSTA_USB_P 33
- CPU_CORE 35
- USB_OTG_M 37
- USB_OTG_P 39

3.3V
C235 10 nF
41
43
PCIE_TX_M 45
PCIE_TX_P 47
49
PCIE_RX_M 51
PCIE_RX_P 53
55
DDR_1.5V
C234 10 nF
57
PCIE_CLK1_M 59
PCIE_CLK1_P 61
AN_1.8V 63

SPI or DIO
- SPI_FRM 65
- SPI_MOSI 67
- SPI_MISO 69
- SPI_CLK 71

73
CPU JTAG Vcc
3.3V 75
77
79

Camera or DIO
- CAM_D3 81
- CAM_D4 83
- CAM_PCLK 85
- CAM_VCLK 87
- MFP_52 89
- MFP_43 91

Console
- DEBUG_TXD 93
- DEBUG_RXD 95

CAN
- DIO_15 97
- DIO_16 99

2 PORT0_ACT_LED
4 PORT0_SPEED_LED
6 RED_LED#
8 GREEN_LED#
10 MFP_105
12 MFP_106
14 MFP_122
16
18
20
22
24
26 MFP_49
28 I2C_CLK
30 I2C_DAT
32 MFP_104
34 AUD_MCLK
36 AUD_CLK
38 AUD_FRM
40 AUD_TXD
42 AUD_RXD
44 CPU_JTAG_TMS
46 CPU_JTAG_TCK
48 CPU_JTAG_TDI
50 CPU_JTAG_TDO
52 ONE_WIRE
54 MFP_51
56 CAM_MCLK
58 CAM_D0
60 CAM_D1
62 CAM_D2
64 CAM_D5
66 CAM_D6
68 CAM_D7
70 CAM_HSYNC
72 CAM_VSYNC
74 USB_OTG_ID
76 USB_5V_LINE
78 UART0_TXD
80 UART0_RXD
82 UART1_TXD
84 UART1_RXD
86 UART2_TXD
88 UART2_RXD
90 UART3_TXD
92 UART3_RXD
94 UART4_TXD
96 UART4_RXD
98 UART5_TXD
100 UART5_RXD

I2C
I2S or DIO
CPU JTAG
Camera or DIO
Serial Ports or DIO

MFP_122 = PWM3
MFP_104 = PWM4

CN2-54 Codec CLK on the TS-8390

MFP_51 has FPGA pin in parallel
** Can use either

Max. load on JTAG_Vcc (CN2-79) is 20 mA
Not always 3.3V

DIO_15 and DIO_16 can be CAN_TXD and CAN_RXD

TYCO_100PIN_MODULE

ETH_CT
C115 .1 uF

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