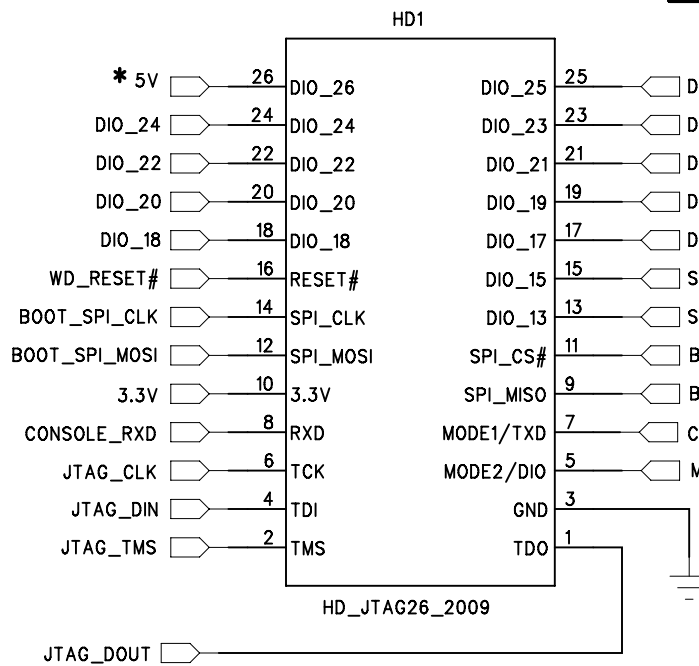


JTAG 26-pin Header

***NOTE: EARLY DESIGNS HAD PIN 26 GO TO DIO_26, BUT ON ALL FUTURE REVS THIS PIN CONNECTS TO 5V**

XP2-5 has:
5K LUTs 2 PLLs
9 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

FPGA with 5000 LUTs



Mode 1	Mode 2	Boots from
1	1	NAND Flash
1	0	SD Card
0	1	Off-board Flash
0	0	Off-board Flash

MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

MODE1 and MODE2 have 4.7K resistor pull-ups on WM-7550

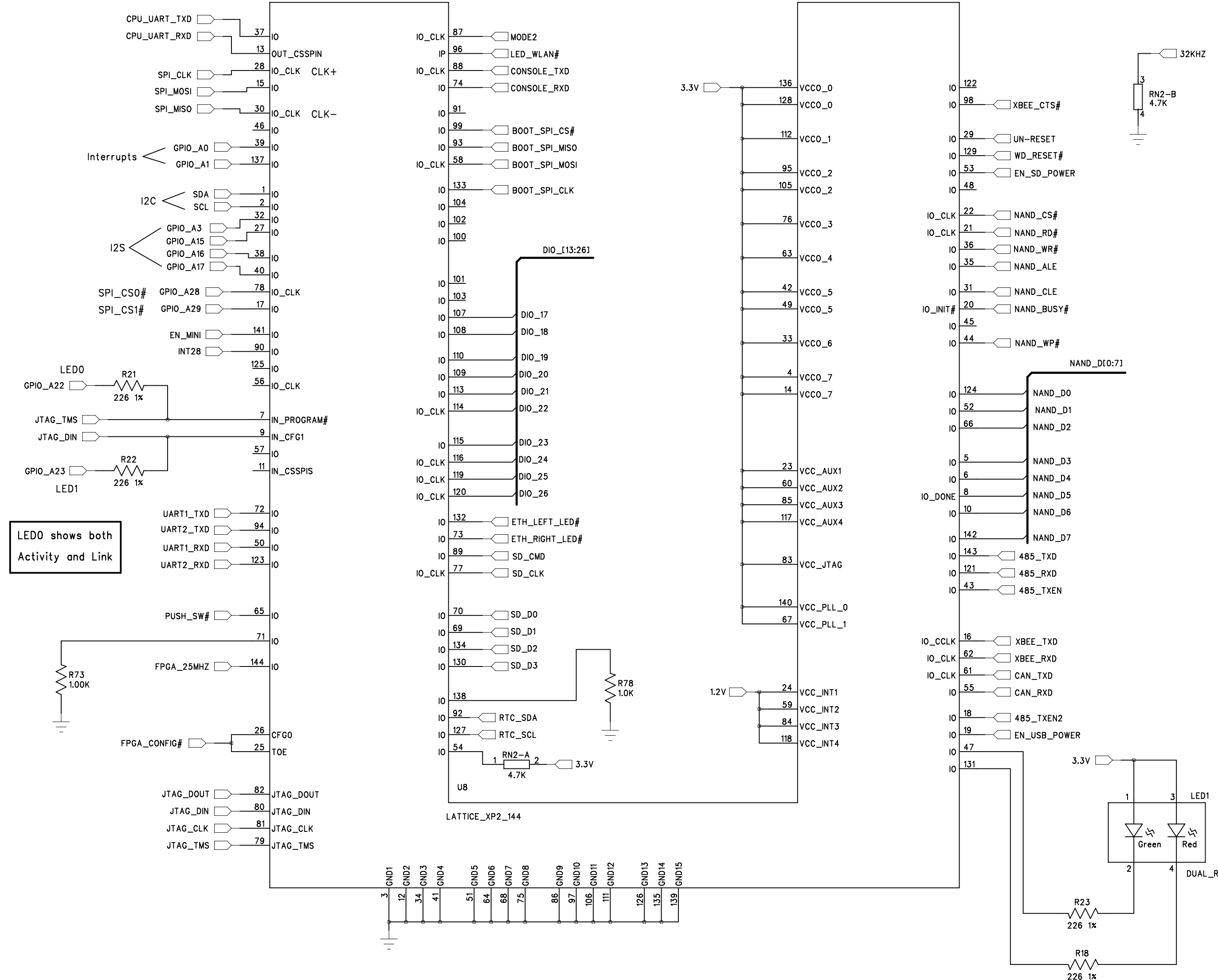
Console always is enabled

Use 680 ohm resistor to GND to set low

LEDO shows both Activity and Link

Board ID bits

	Pin 54 (weak PU)	Pin 138 (weak PD)	Pin 71	Pin 37	Hex
TS-7500	1	1	1	1	F
TS-7550	1	1	0	1	B
WM-7551	0	0	1	1	C
TS-7552	1	0	1	1	D
TS-7553	1	0	0	1	9
TS-7554	0	0	0	1	8
TS-7555	0	1	0	1	A
TS-4500	0	0	0	0	0



UN-RESET rising edge, deasserts CPU Reset (Must be careful at start up) It has a PD resistor -- always keep low
EN_SD_POWER should initialize high

During JTAG Flash programming the PROGRAM# pin should be high else it can inhibit Flash --> SRAM
DONE likewise must be high These do have weak PU resistors

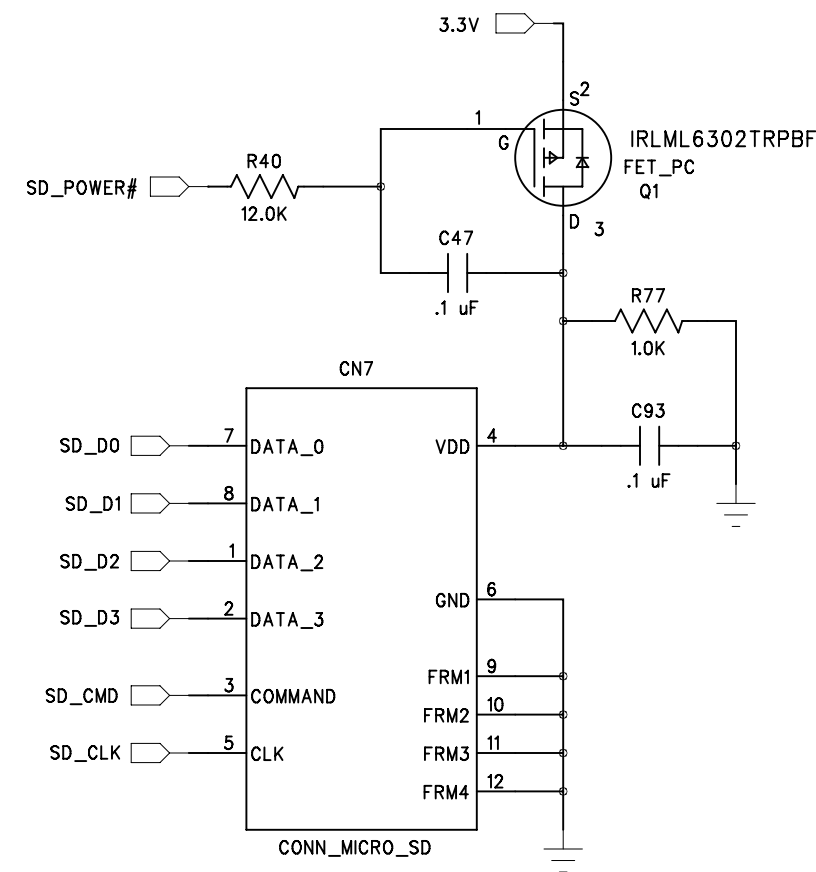
PROGRAM#, DONE, and INIT# are dedicated configuration pins when CFG0 is low. When CFG0 is high they are "general purpose I/O"
Page 4 of TN1141

Set CONFIG_MODE to NONE This allows all pins to be used

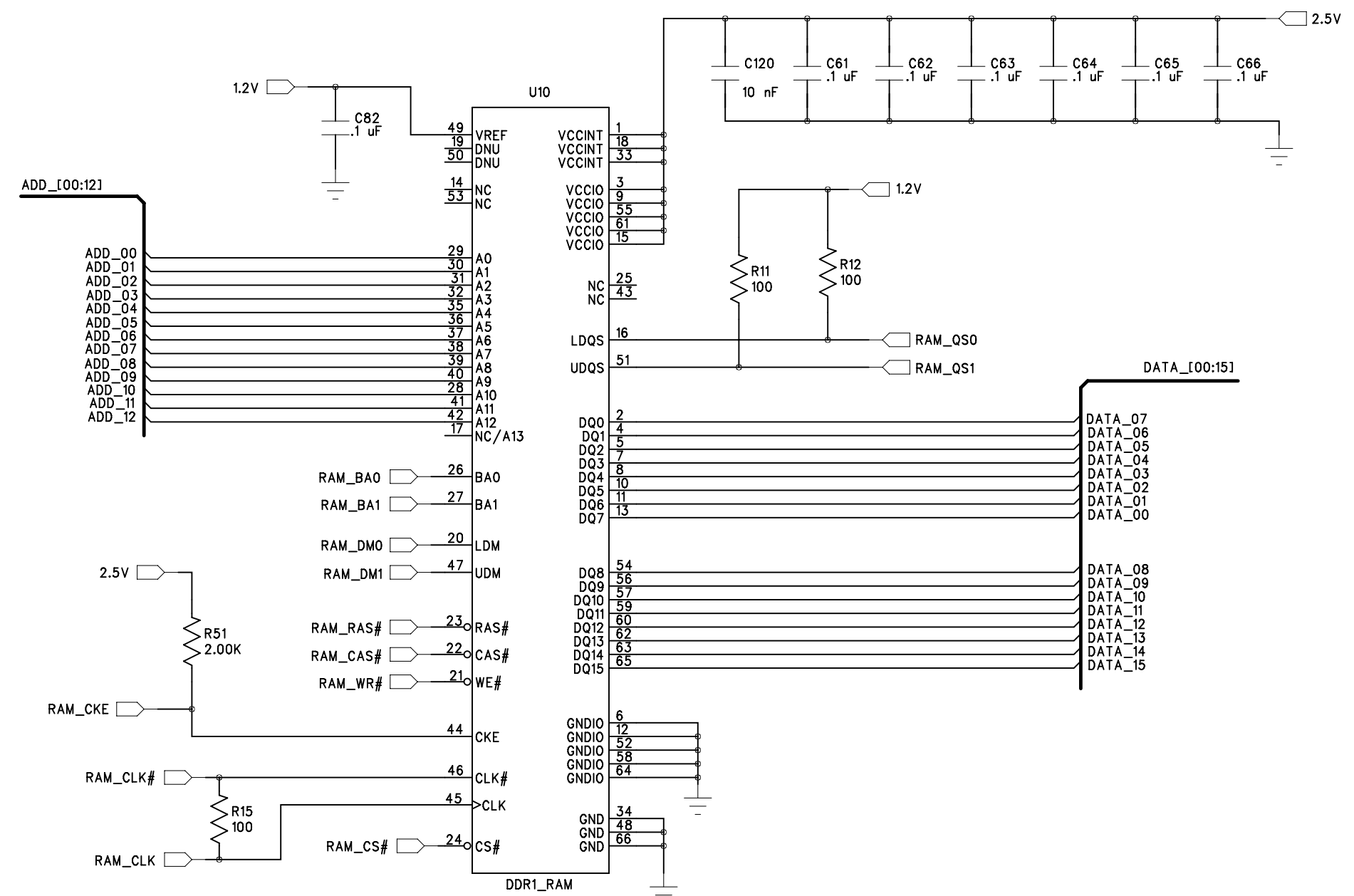
Pull-up and pull-down resistors are 6 to 30K ohms

Page 37 of Data Sheet (Hot Socketing) Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling

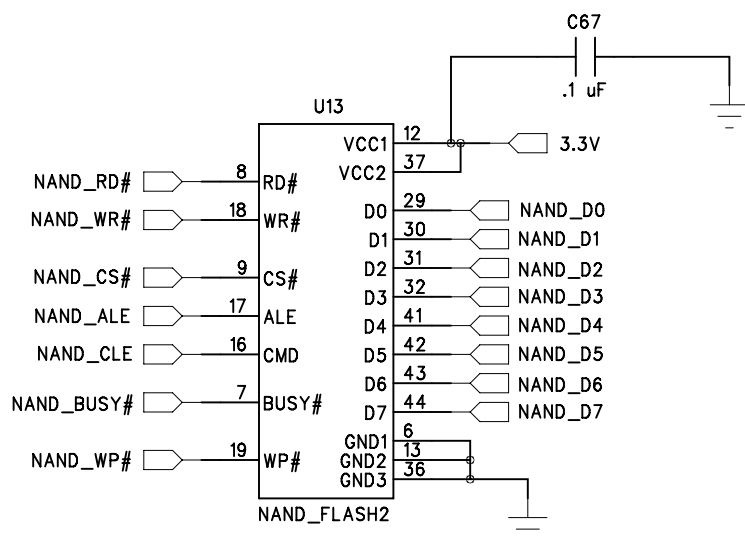
Micro SD Card Socket



64 Mbyte DDR1 SDRAM



512 Mbyte NAND Flash



DDR RAM Notes

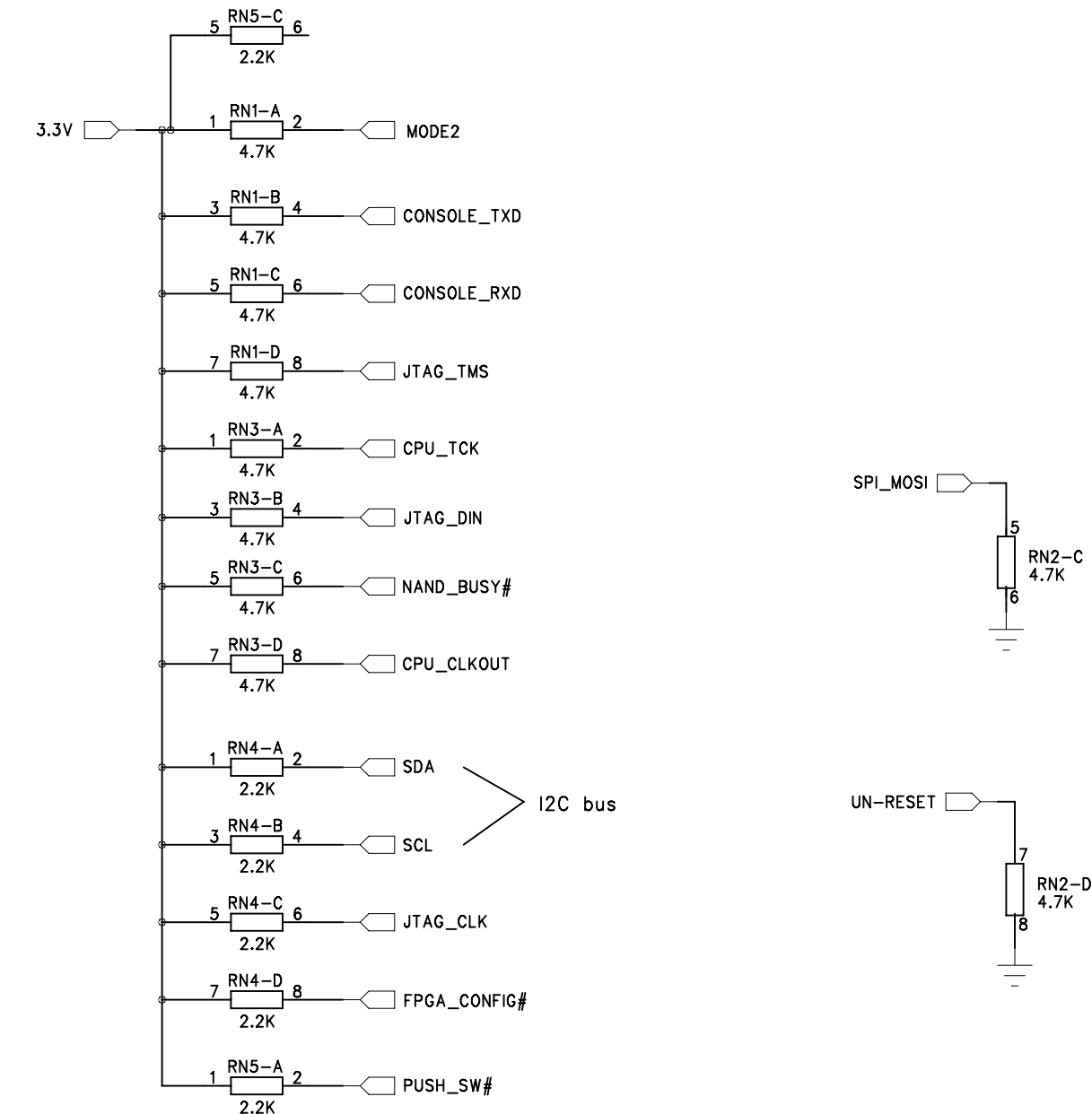
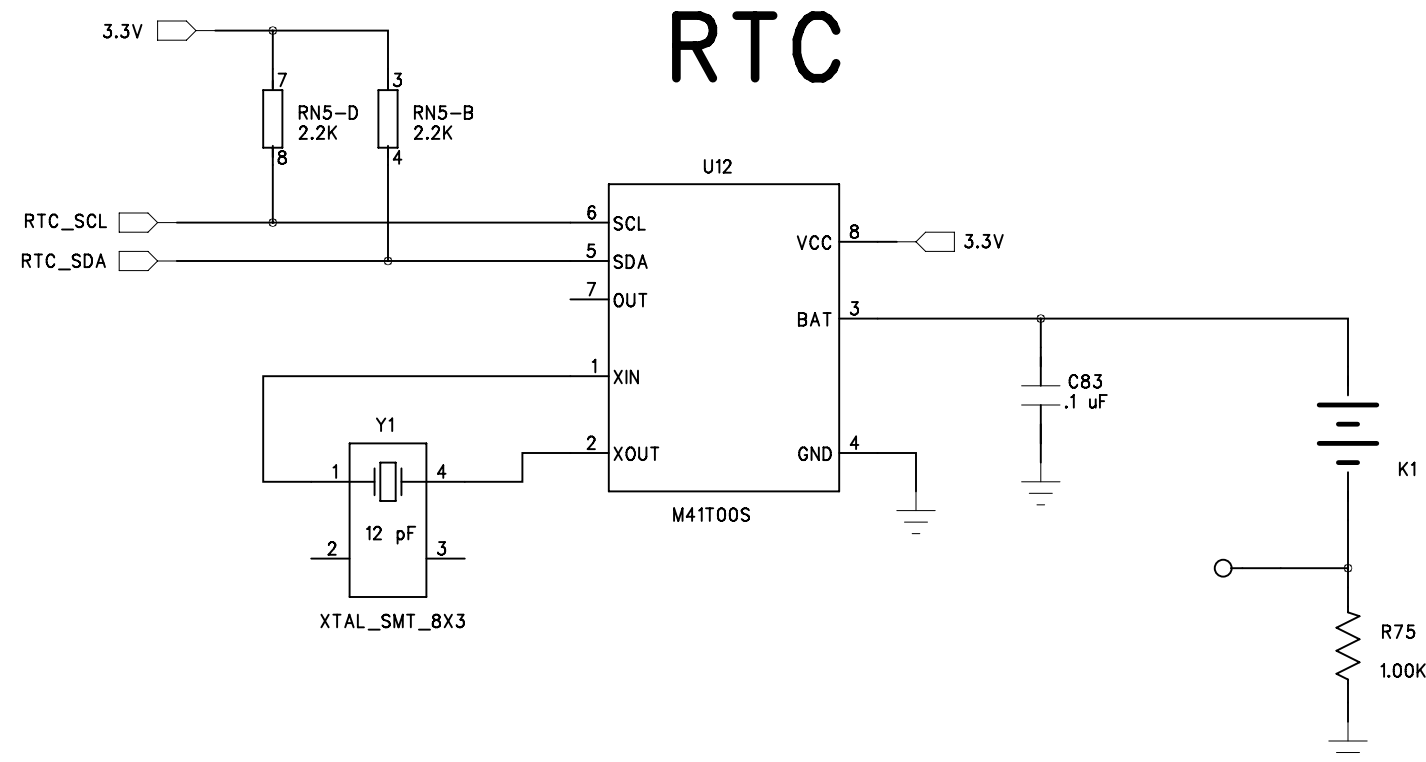
The DDR clock differential pair is the most critical trace on the entire board

The data lines in each byte lane can be swapped on the RAM chip for optimal layout
Example: D0 and D5 can be swapped, but not D7 and D8

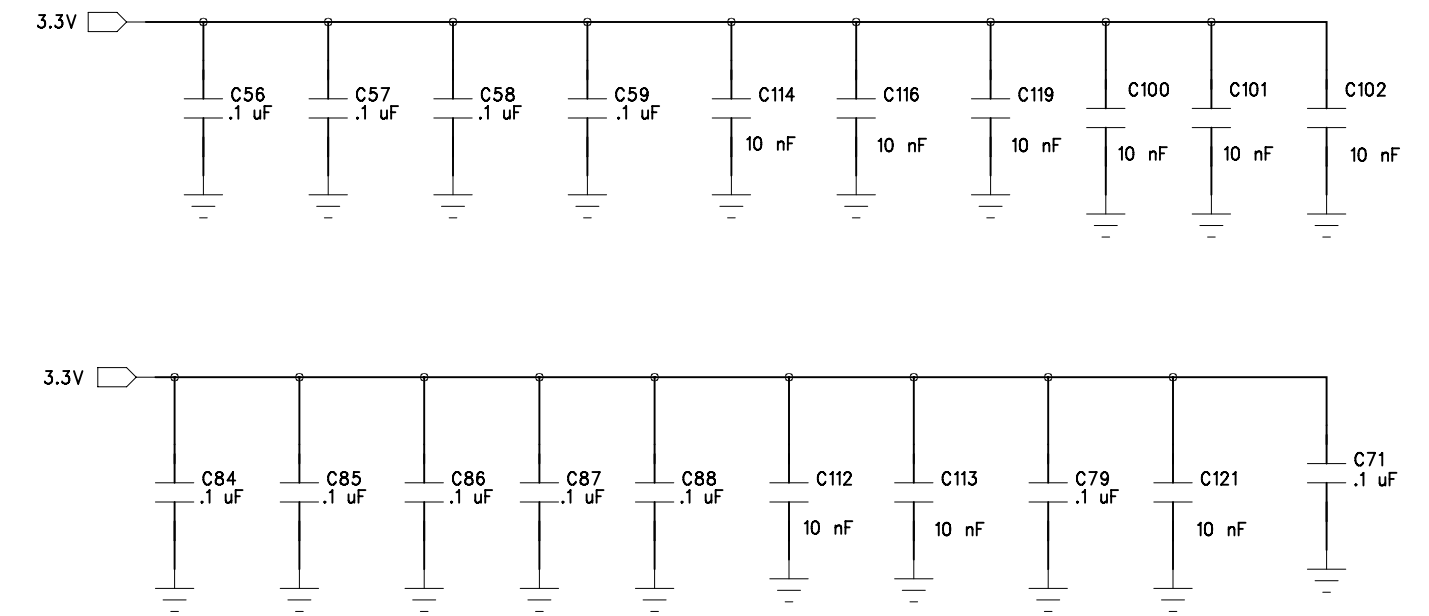
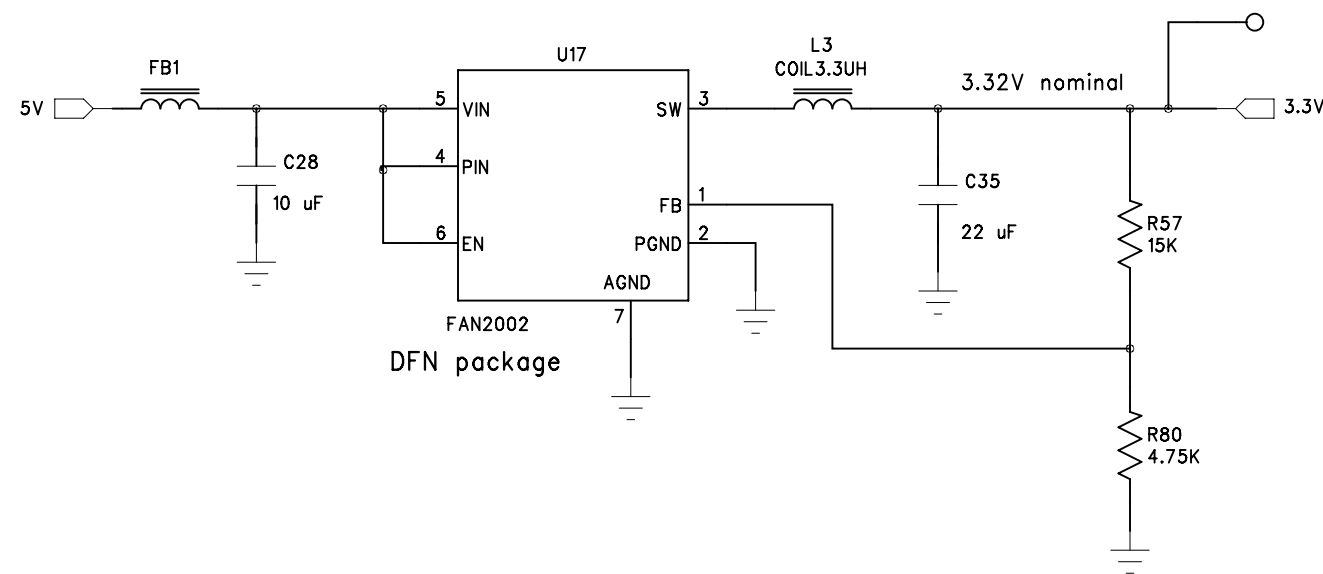
The trace length of each data line (in a single byte lane) and the respective QS and DM signals must be matched to within 2.5 mm

Address and Command signals can be grouped together, but must be isolated from data and M_DSQ and M_DM signals (by at least .5 mm)
Or run them on different layer

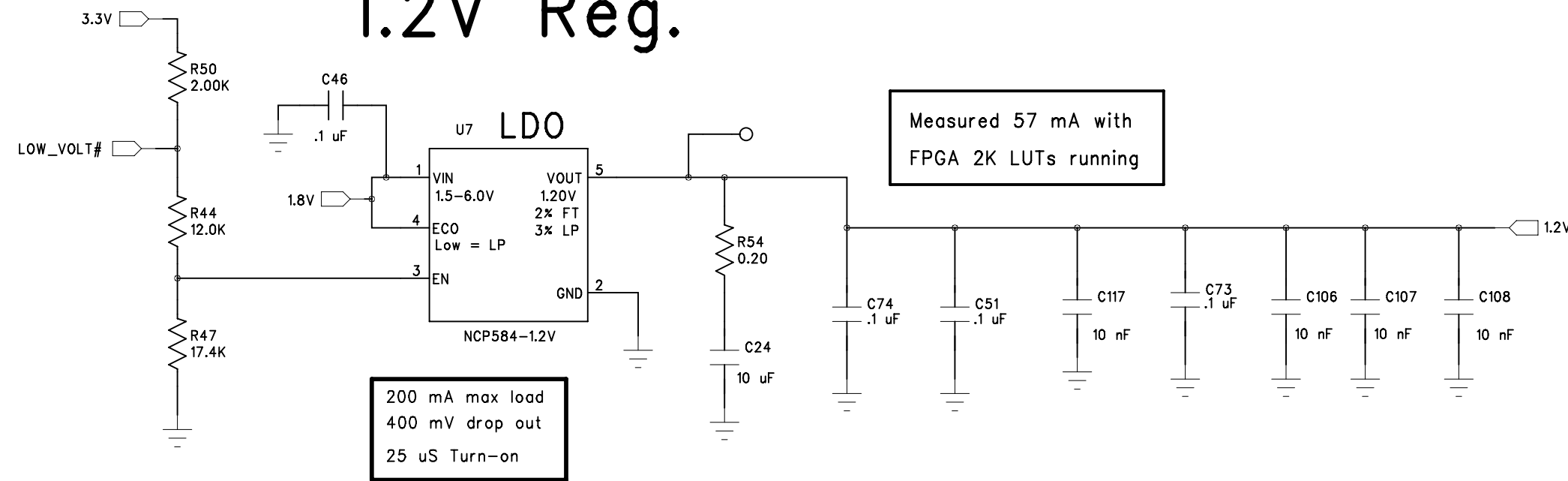
RTC



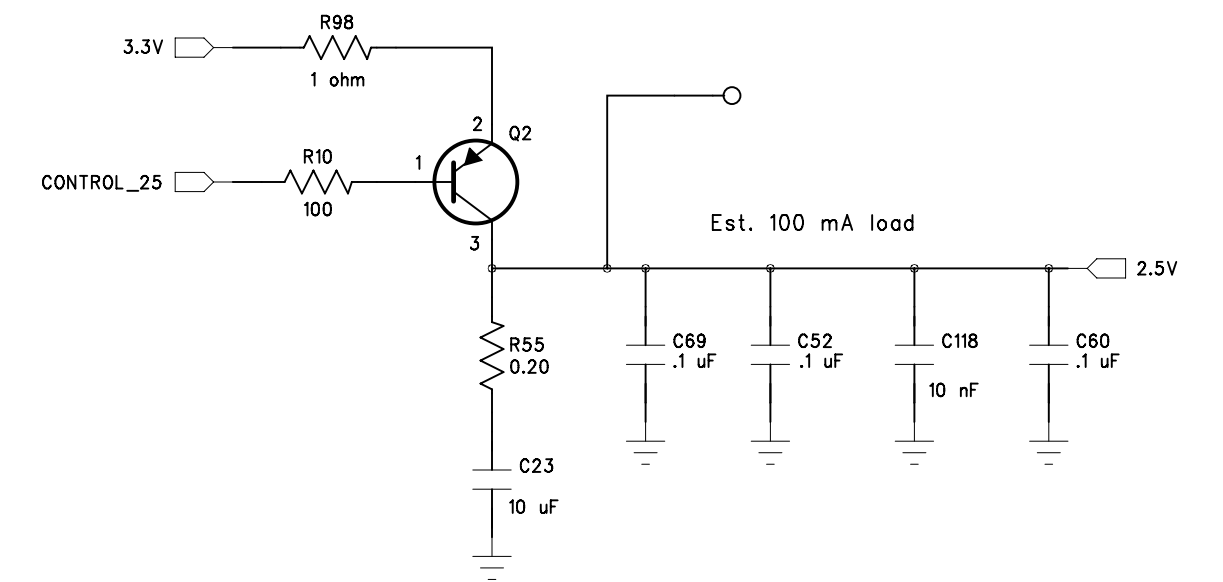
3.3V Regulator



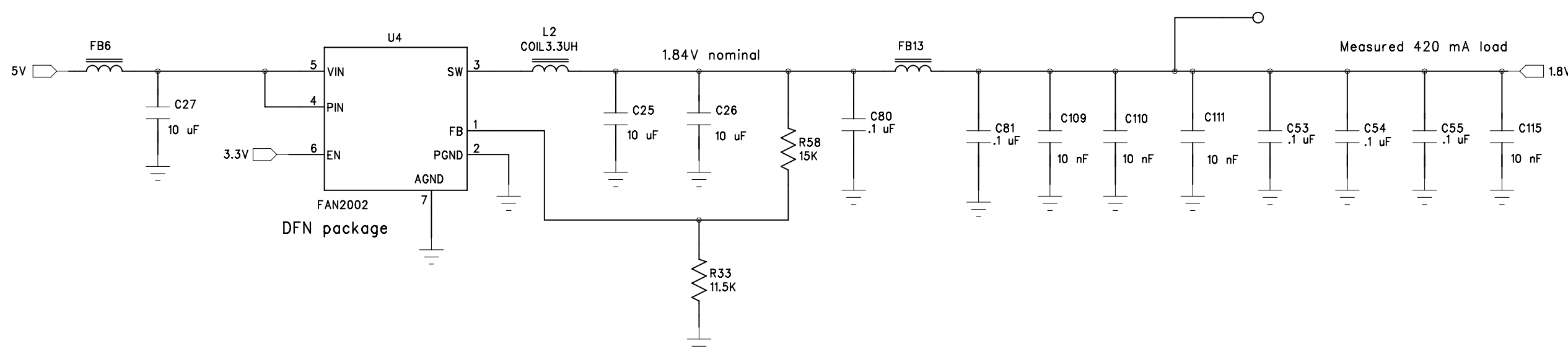
FPGA Core 1.2V Reg.



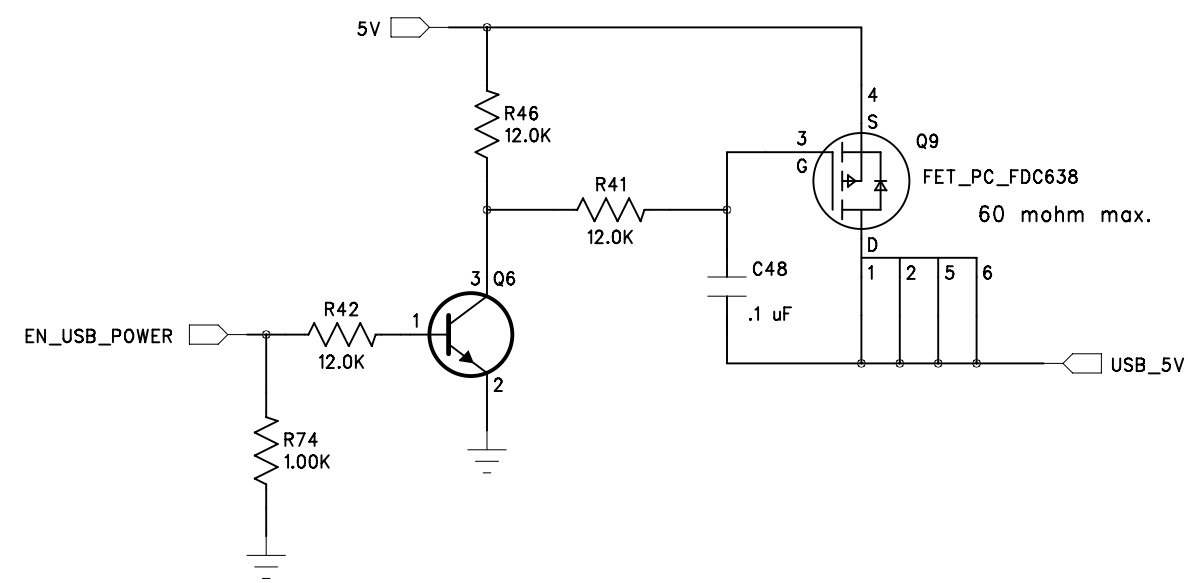
2.5V Regulator



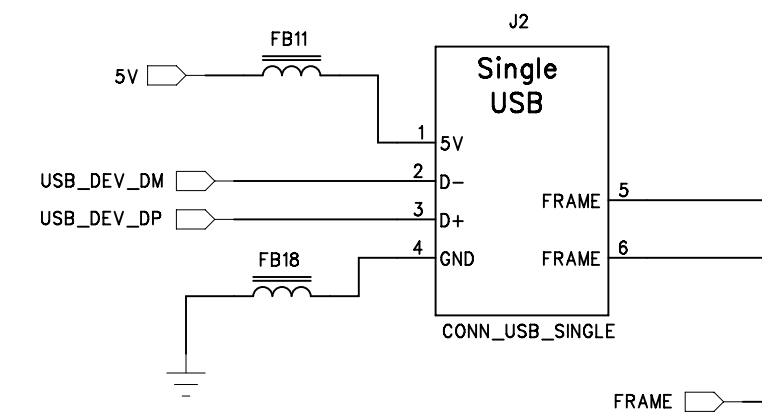
1.8V Regulator



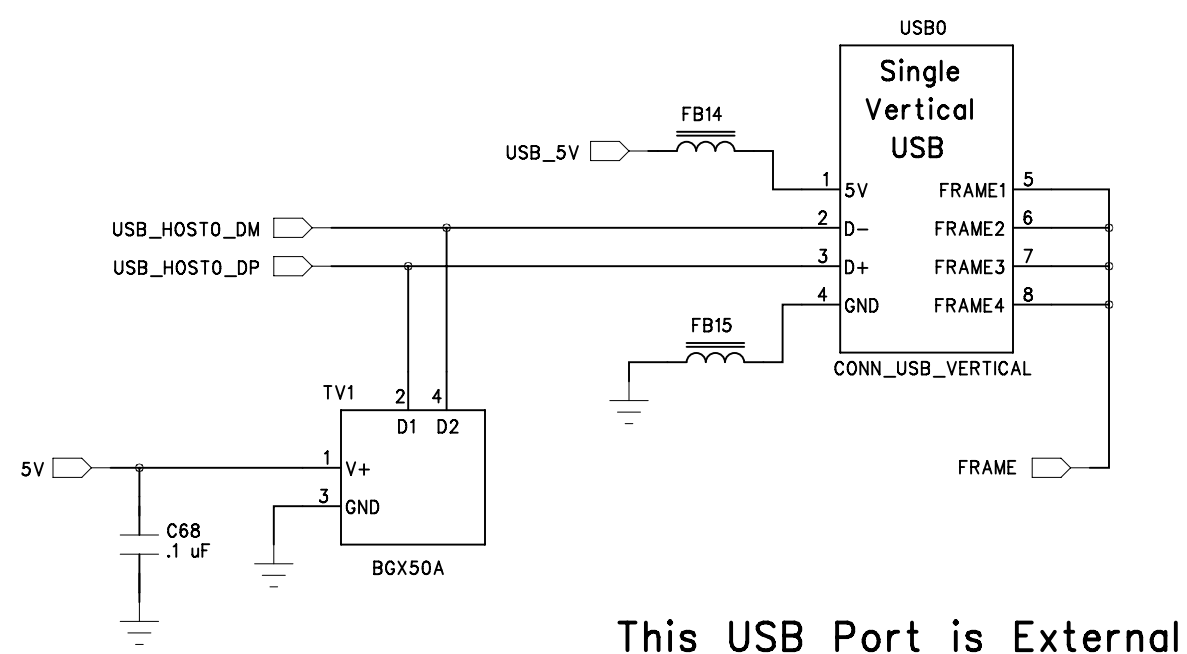
USB Power Switch



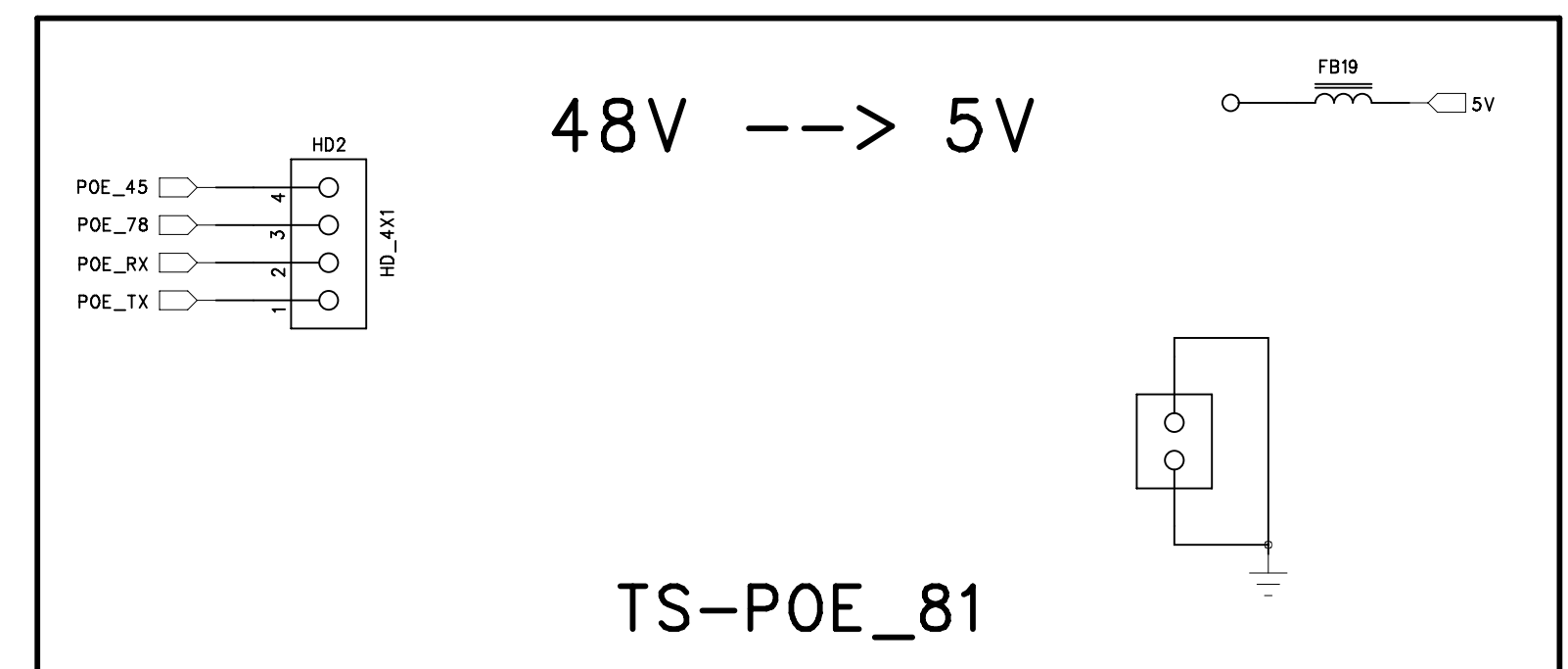
USB Device Port



USB Host 0



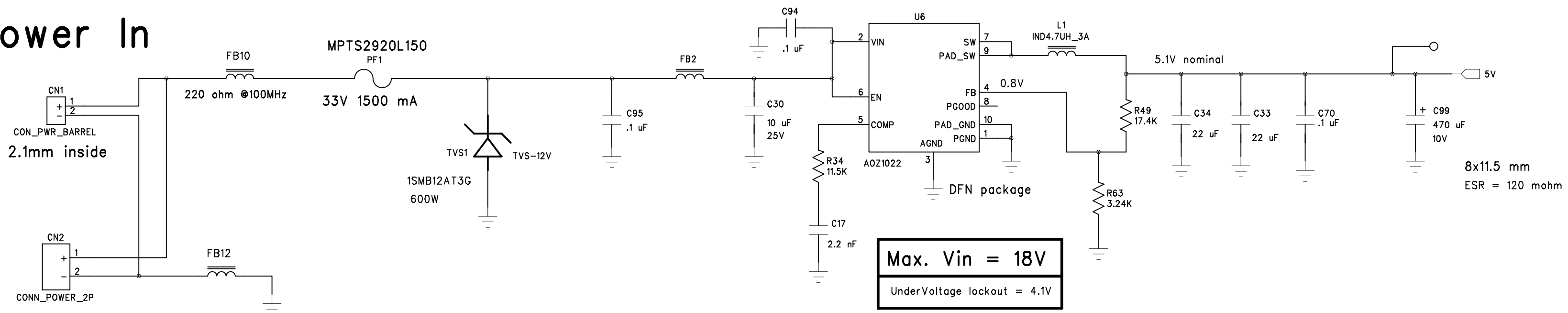
POE Power option



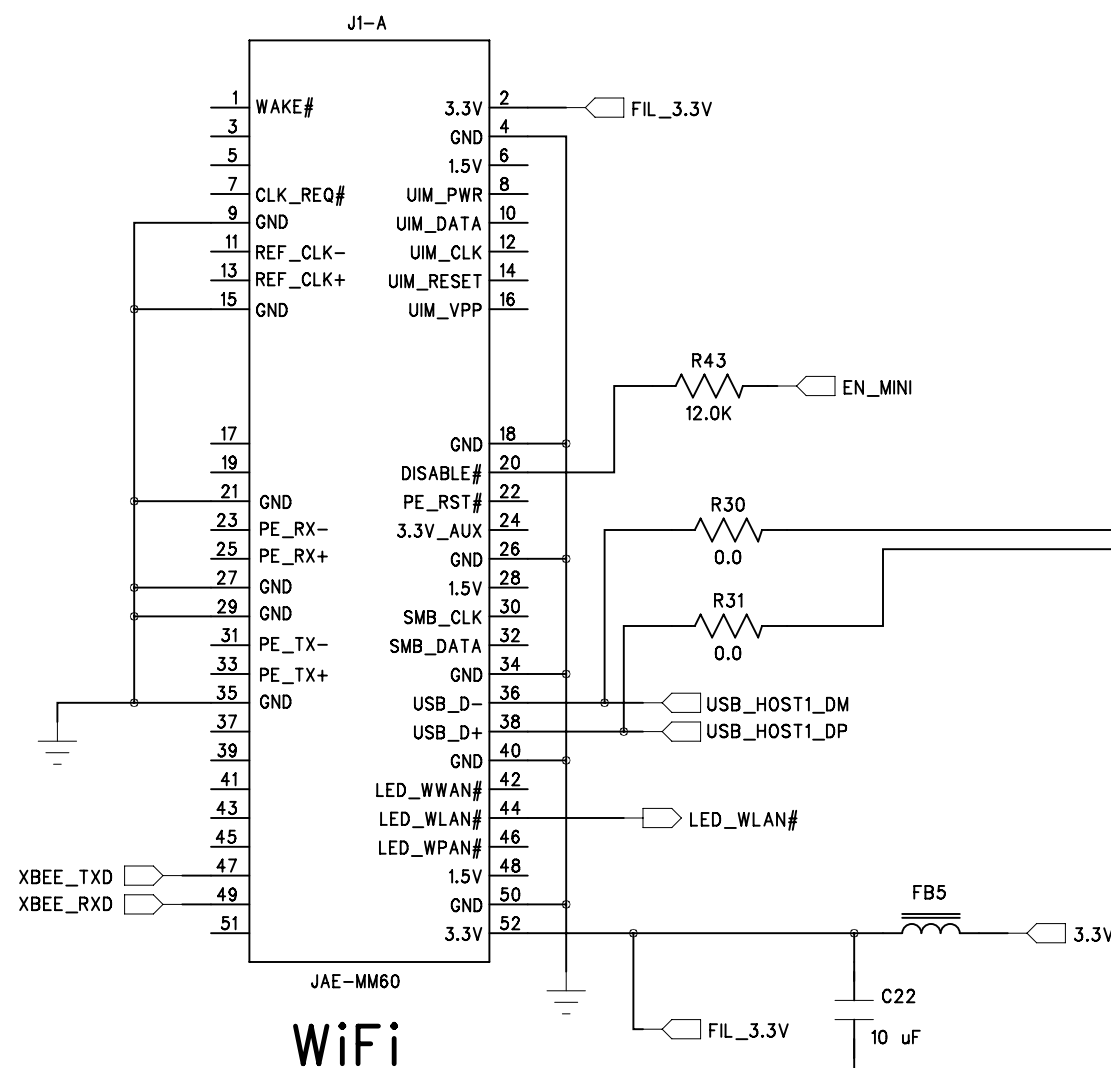
Technologic Systems	Date Feb. 24, 2010
Title: TS-7553 USB, POE module	
Rev:	Designer
	Sheet 5 of 7

5V-12V Power In

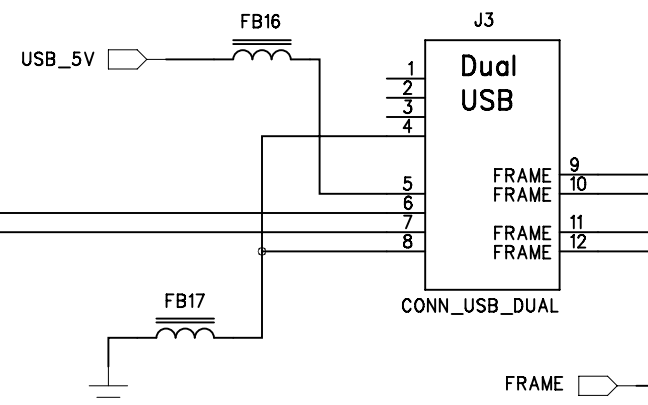
5.0V Power Supply up to 2500 mA



Mini PCIe Socket



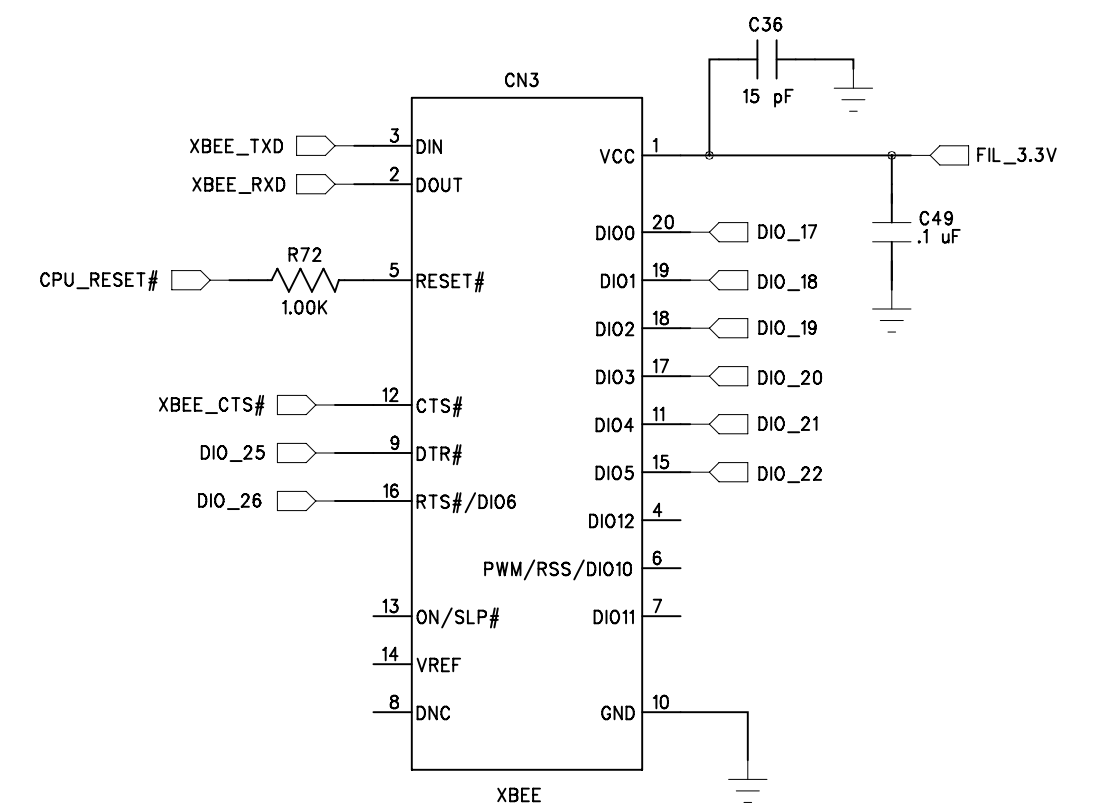
USB (Internal) for WiFi Dongle



Force Boot to SD card



Digi/MaxStream ZigBee Radio



Reset# must be driven with Open drain

CTS# is an output that can be used for hardware flow control

Baud rates up to 230.4K supported

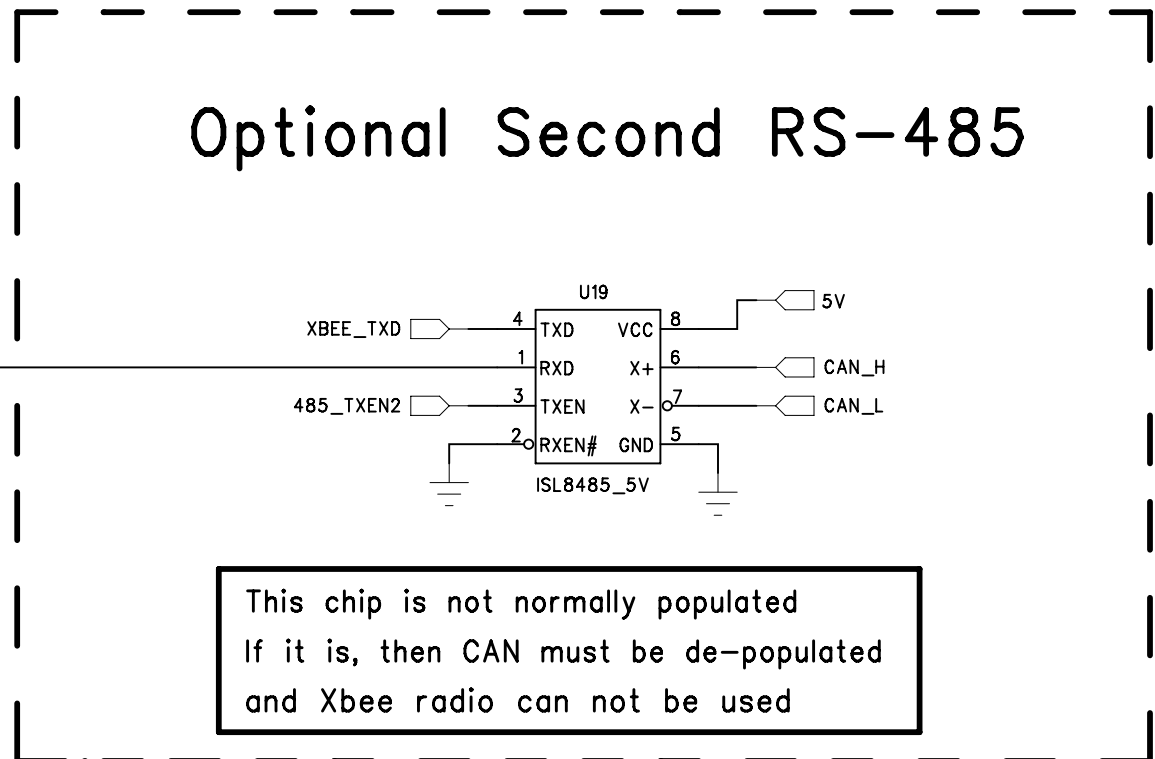
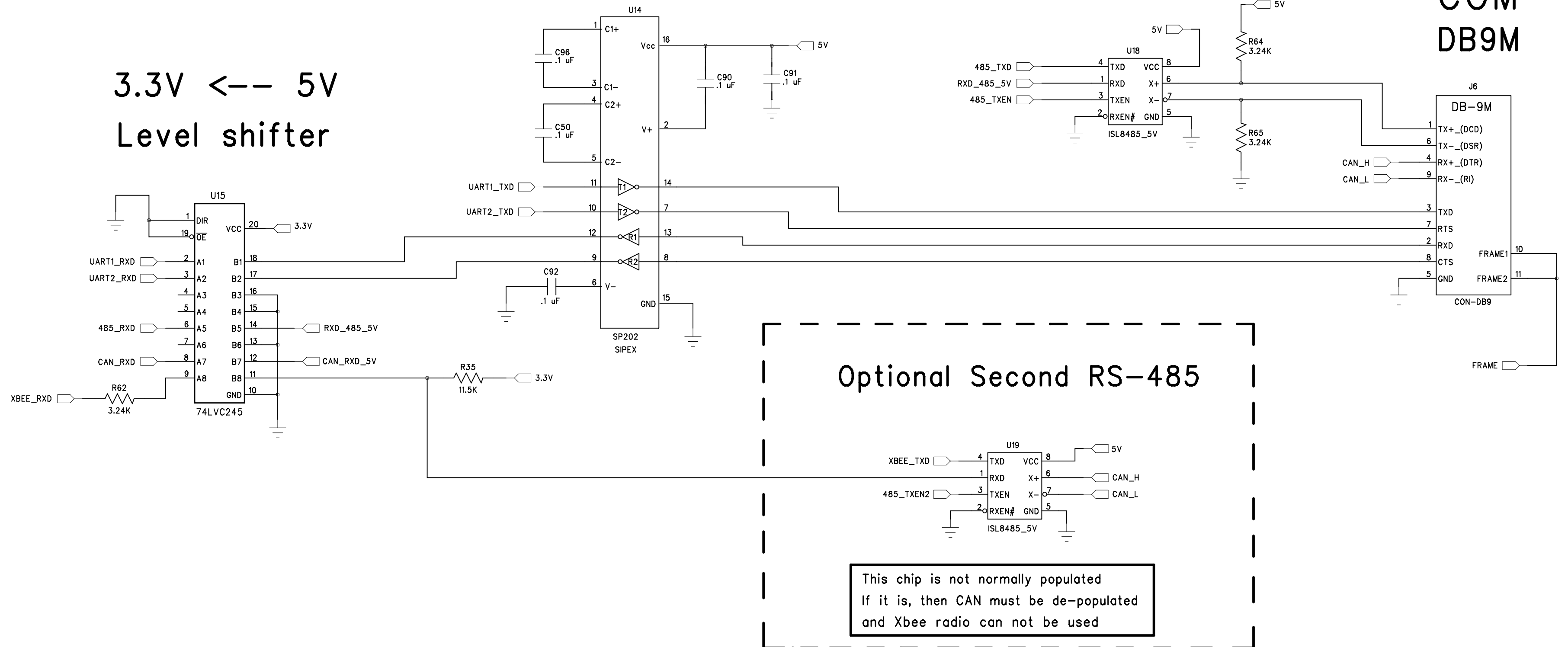
RTS# and DTR# are inputs that are needed for reprogramming the Xbee

RS-232 Transceiver

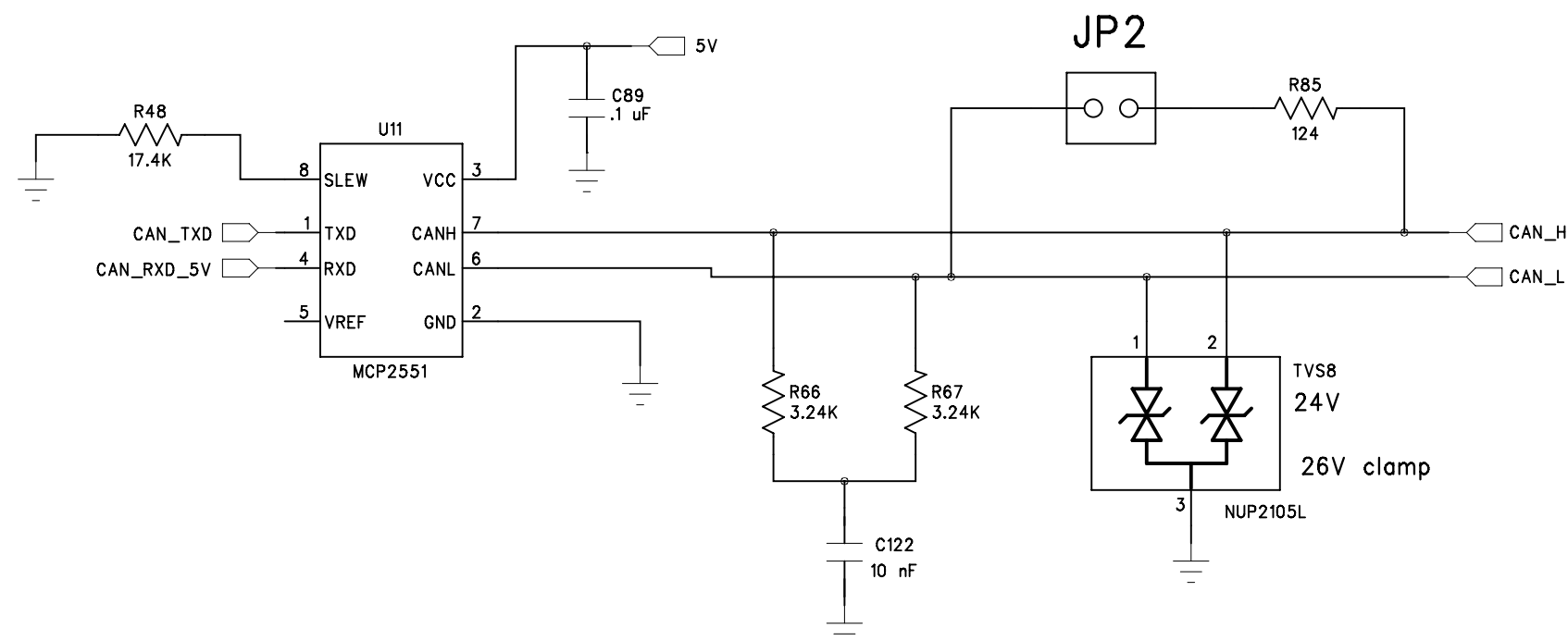
RS-485 Driver

COM DB9M

3.3V <-- 5V
Level shifter



CAN Tranceiver



Temp Sensor

