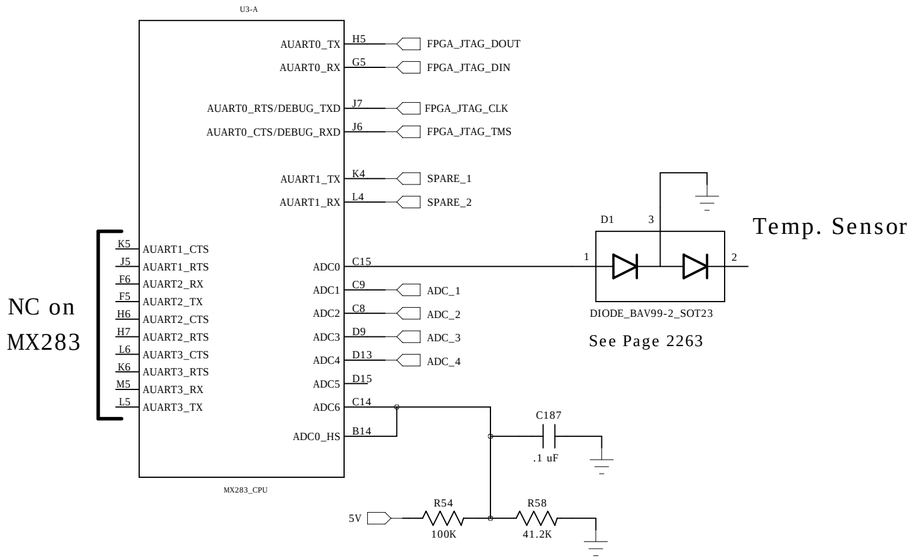
MX283 ARM9 CPU

UARTs, ADC



NC on MX283

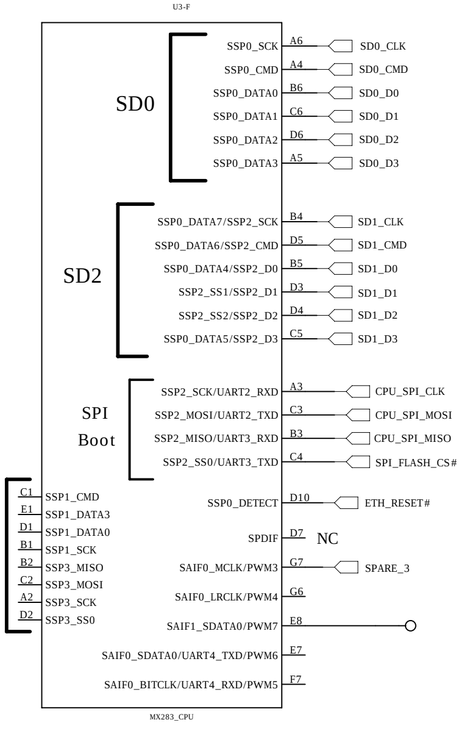
Temp. Sensor

See Page 2263

Audio

SD Card

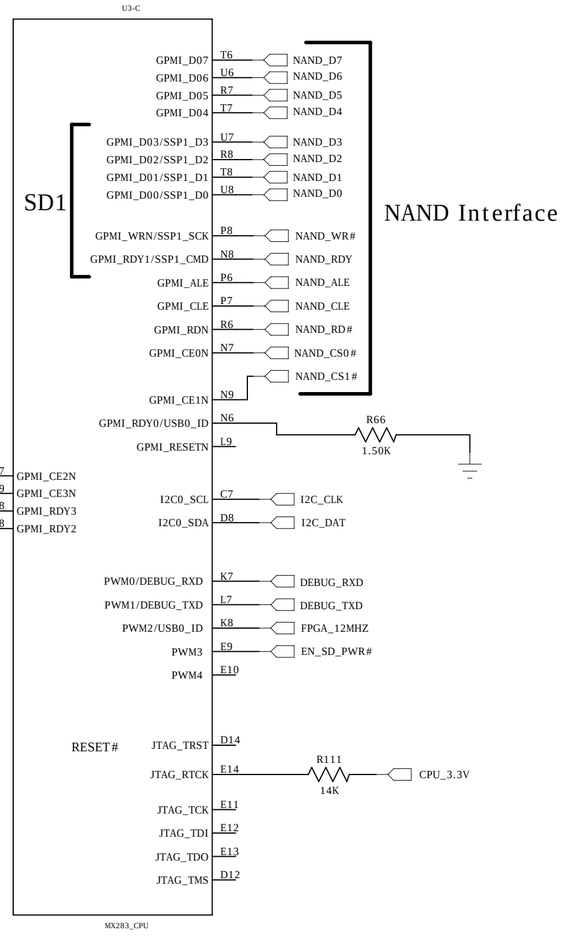
SPI Boot



NC on MX283

NAND, PWM

JTAG, I2C



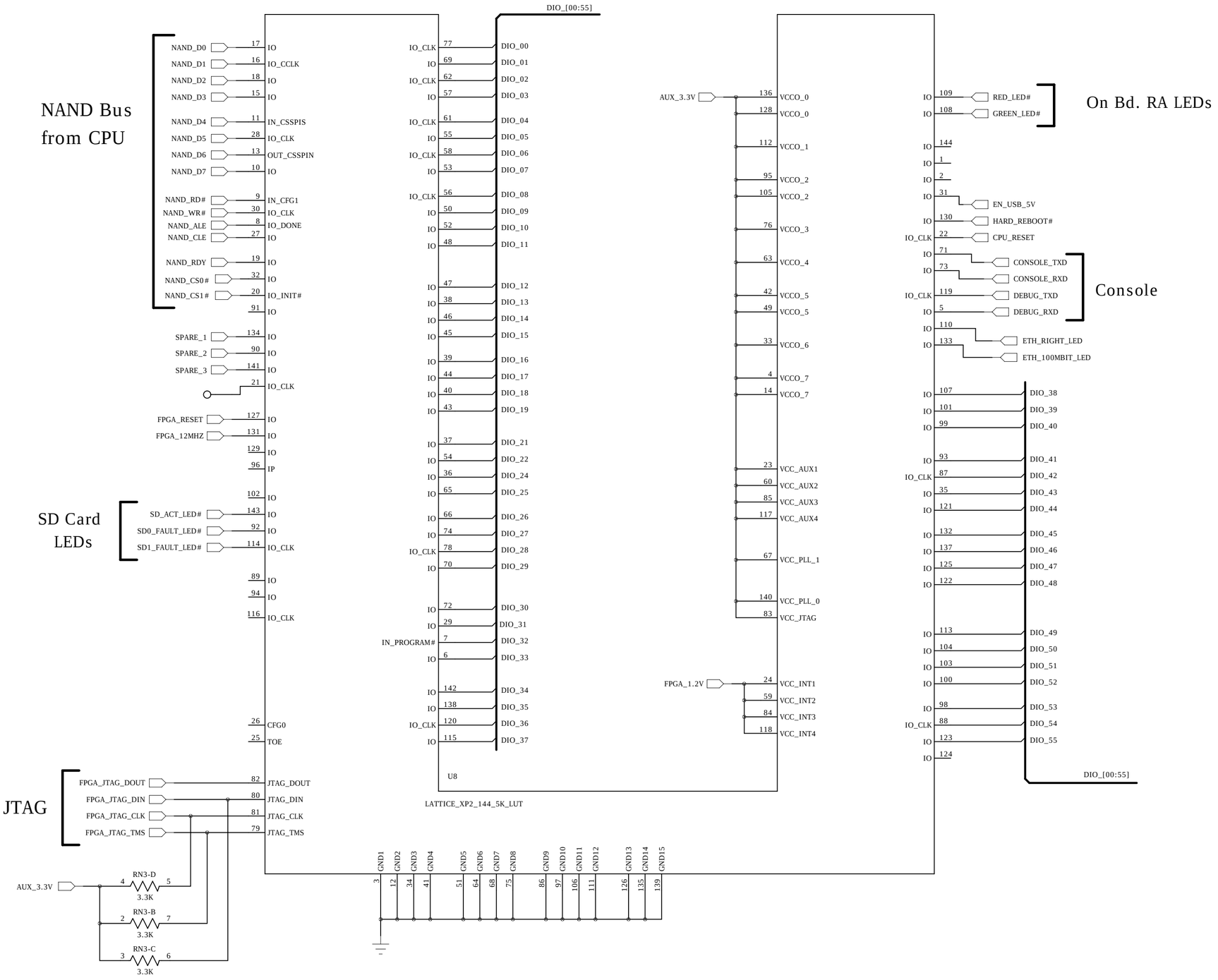
NC on MX283

NAND Interface

All JTAG have 47K internal PU except RTCK

Technologic Systems		Date Feb. 28, 2013
Title: TS-7600 MX283 CPU		
Rev: A	Designer	Sheet 1 of 6

FPGA with 5K LUTs



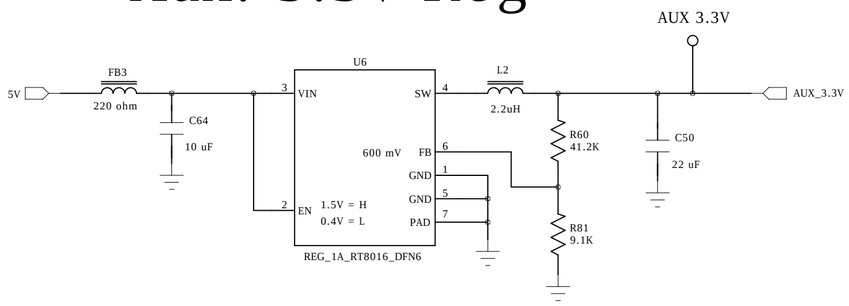
XP2-5 has:
5K or 8K LUTS 2 PLLs
9/12 blocks of 1Kx18 Block RAM
12 18x18 Multipliers
100 I/O with 144 pin package
"instant ON" = about 1.5 mS
input PLL clock = 10 MHz min

Pull-up and pull-down resistors are 6 to 30K ohms

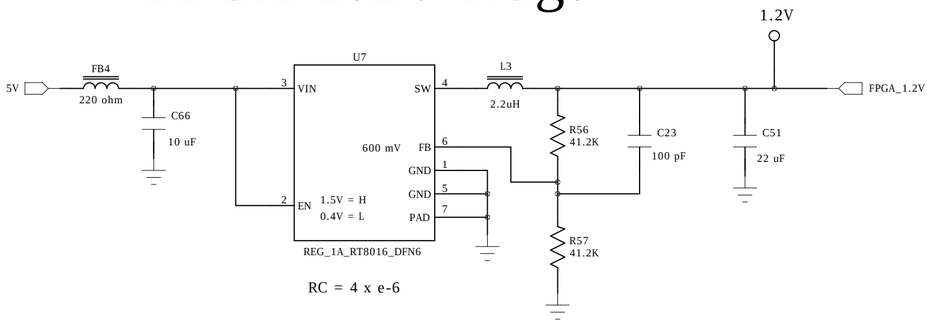
Page 37 of Data Sheet (Hot Socketing)
Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling

Technologic Systems		Date Feb. 28, 2013
Title: TS-7600 FPGA		
Rev: A	Designer	Sheet 2 of 6

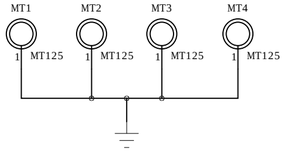
Aux. 3.3V Reg



FPGA 1.2V Reg.

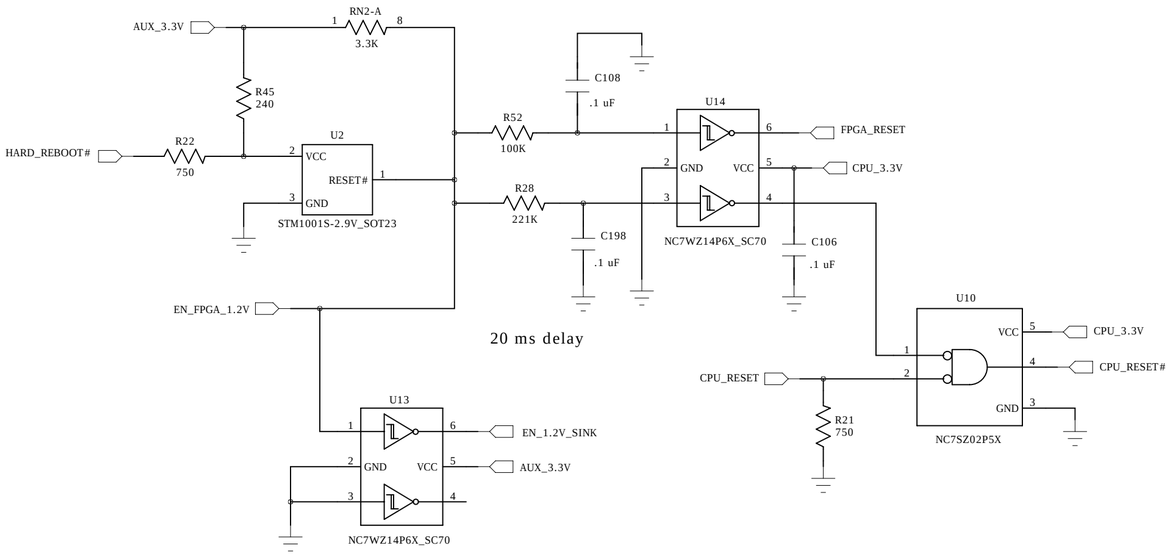


GND Test Point

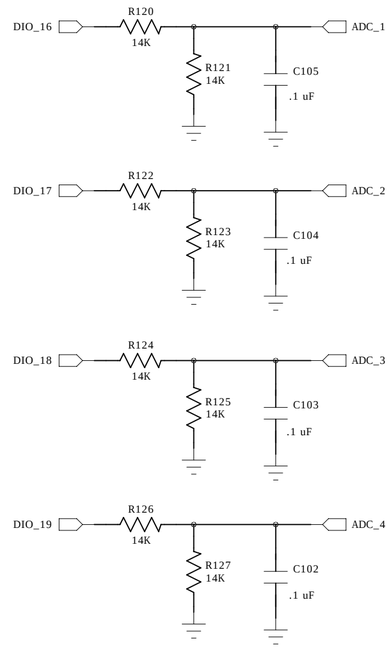


Technologic Systems	Date Feb. 28, 2013	
Title: TS-7600 Power Reg. and Boot Straps		
Rev: A	Designer	Sheet 3 of 6

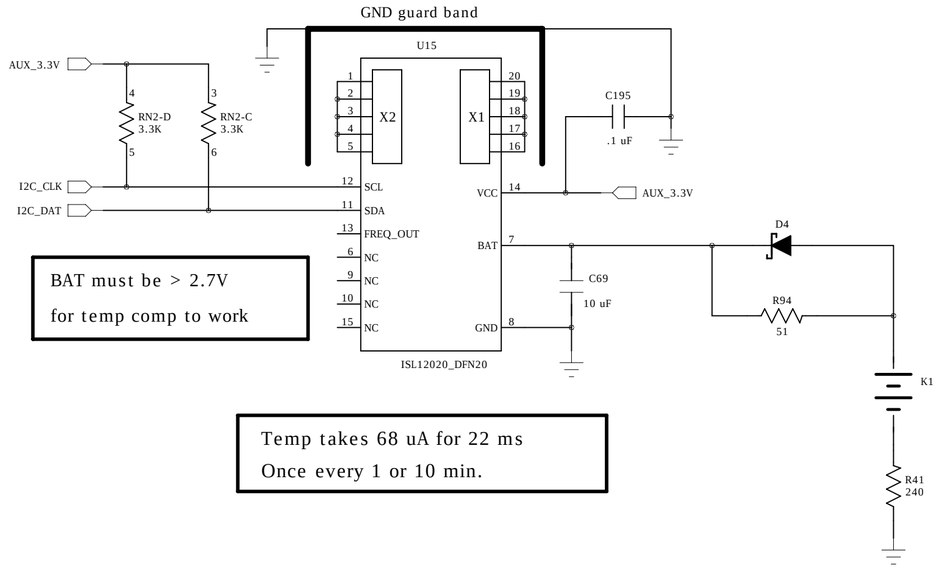
RTC and Reset Sequencer



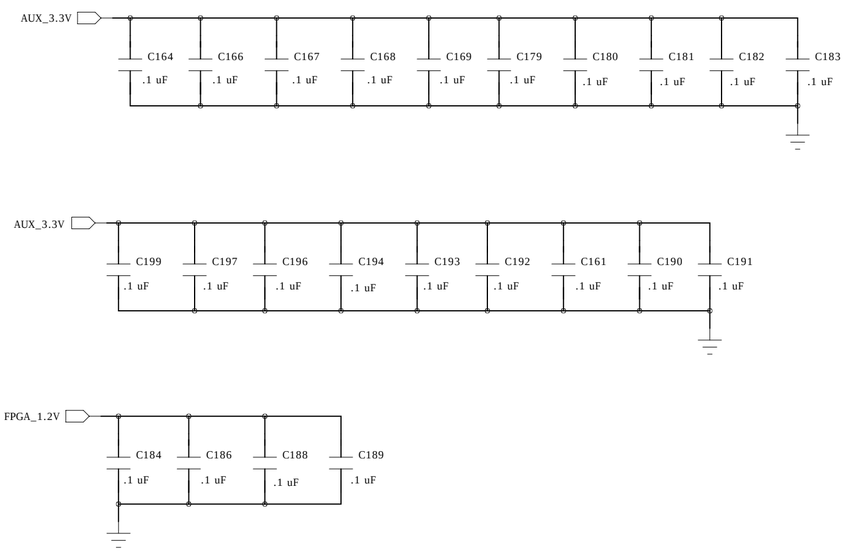
Analog Inputs



RTC and Temp. Sensor

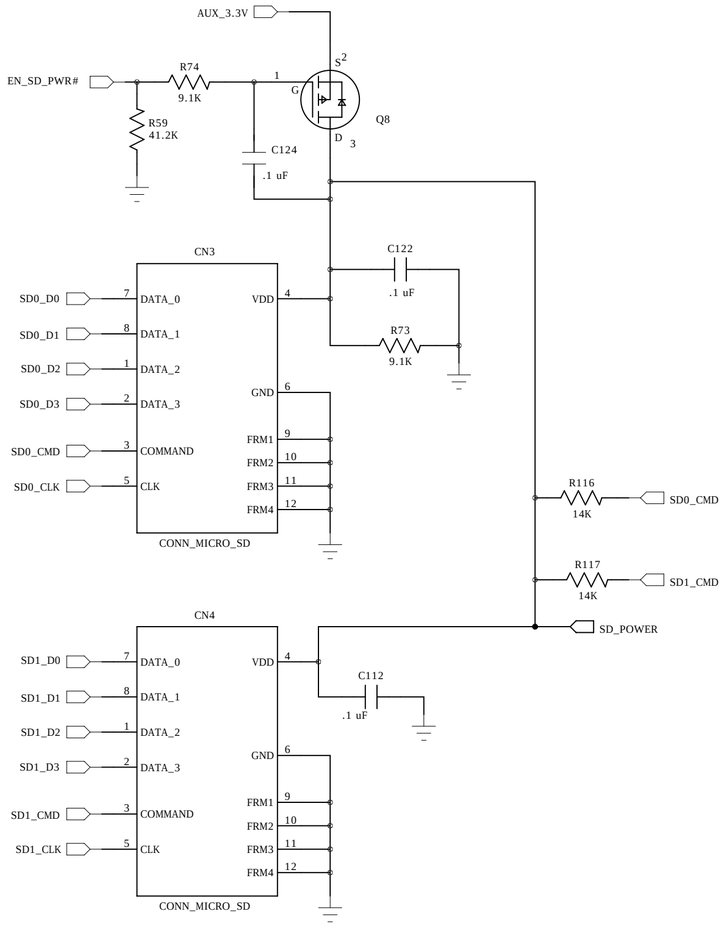


FPGA Bypass Caps

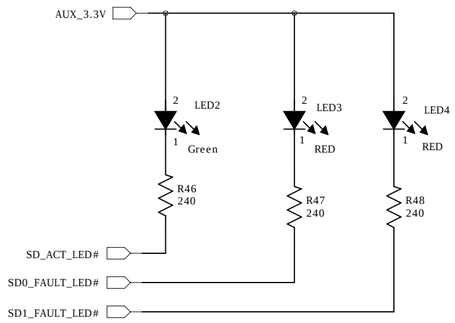


Technologic Systems	Date Feb. 28, 2013	
Title: TS-7600 Boot Flash, RTC, Reset		
Rev: A	Designer	Sheet 4 of 6

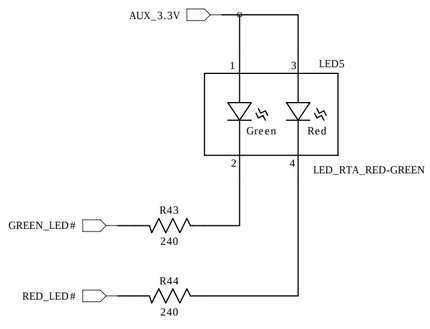
Micro SD Card Sockets



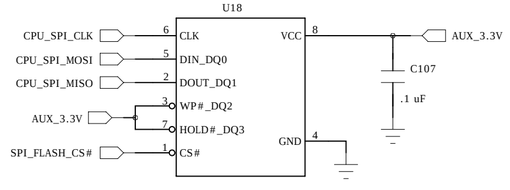
SD LEDs



Red/Green LEDs



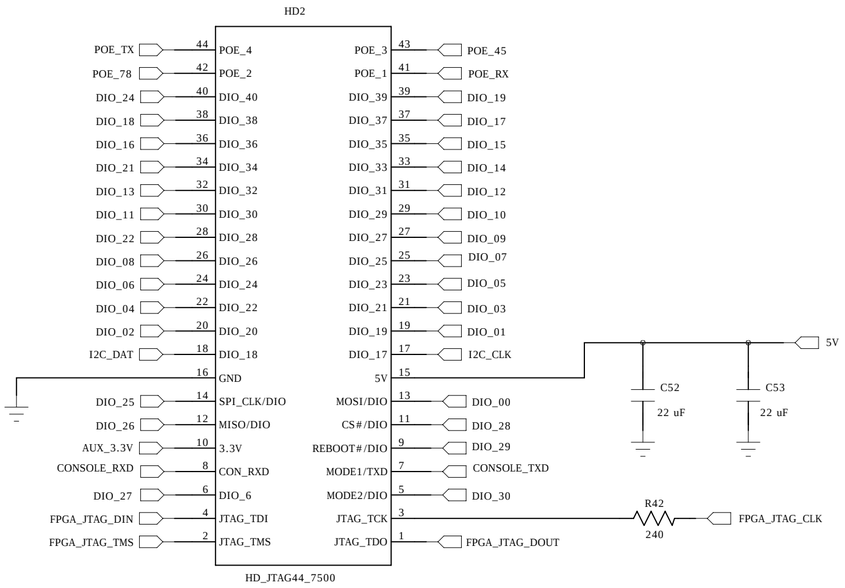
SPI Boot Flash



64 bytes of OTP

Technologic Systems		Date Feb. 28, 2013
Title: TS-7600 SD Card		
Rev: A	Designer	Sheet 5 of 6

44-Pin DIO Header



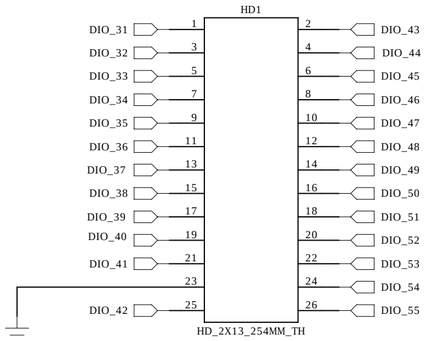
MODE1 and MODE2 states are latched when CPU_RESET# is deasserted

Logic "0" on MODE2 signal forces Boot from SD card

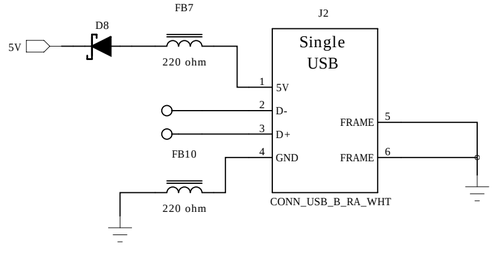
MODE1 and MODE2 have 4.7K resistor pull-ups on TS-7500

Logic "0" on MODE1 forces Console onto the TXD and RXD lines

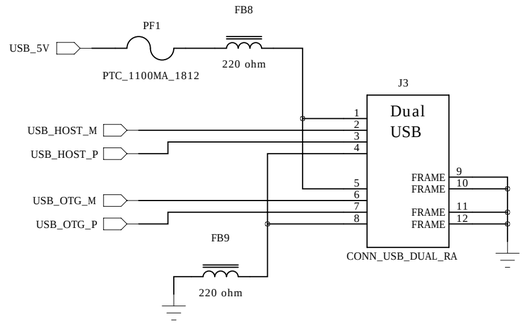
26-Pin DIO Header



USB Device Port



USB Host Ports



Technologic Systems		Date Feb. 28, 2013
Title: TS-7600 44-pin DIO and USB		
Rev: A	Designer	Sheet 6 of 6