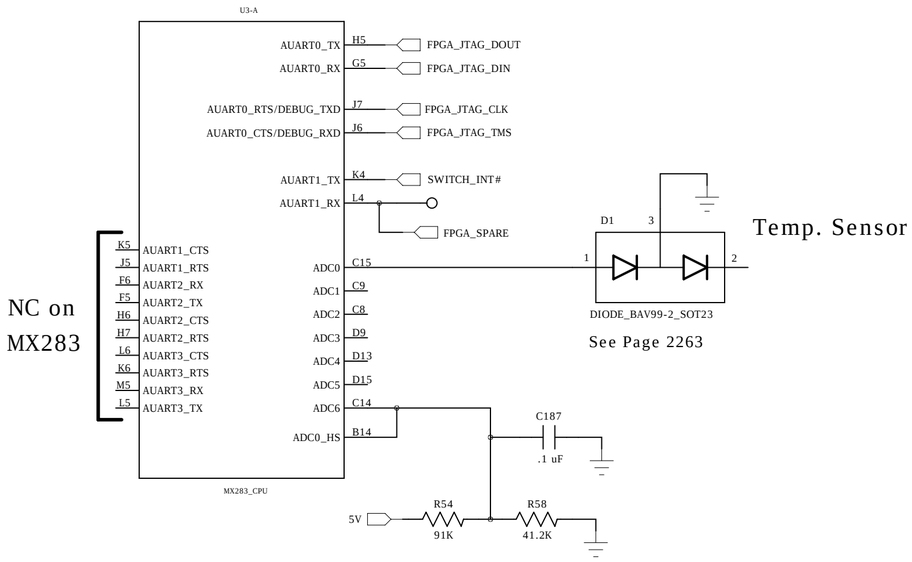
MX283 ARM9 CPU

UARTs, ADC



NC on MX283

D1 DIODE_BAV99-2_SOT23

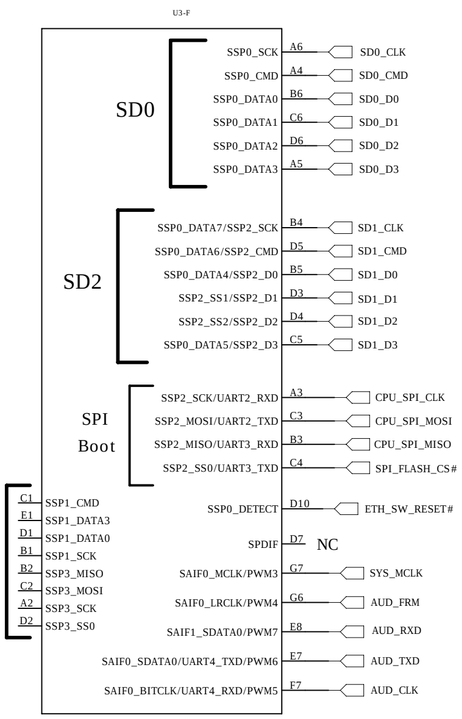
Temp. Sensor

See Page 2263

Audio

SD Card

SPI Boot



NC on MX283

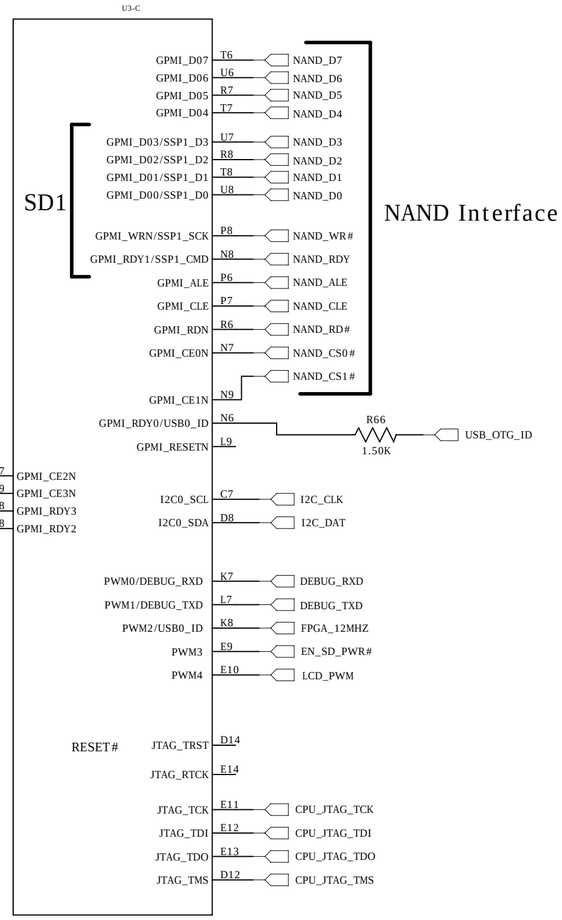
12 MHz default boot clock
Max SPI clock rate = 20 MHz

U3.D3 and U3.D4 are extra
2 data lines for SPI x4 read
Page 1313 of Data sheet

Page 1311 - Winbond SPI x2 and x4 supported
EVK schematic references a 8Mbit Winbond chip

NAND, PWM

JTAG, I2C



NC on MX283

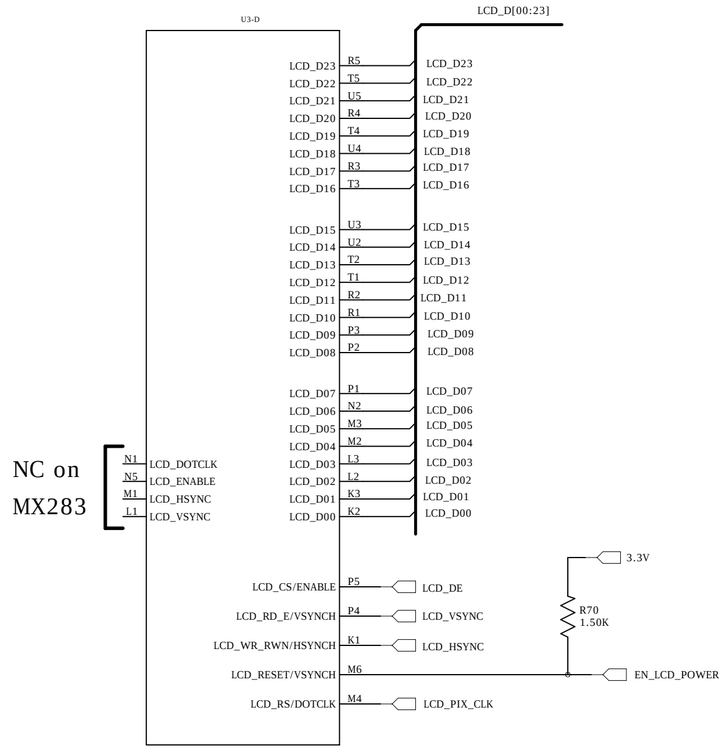
SPI

SCK = CLK
CMD = MOSI
D0 = MISO
D3 = CS#

NAND Interface

All JTAG have 47K internal PU except RTCK

LCD



NC on MX283

LCD_00 thru LCD_04
Control Boot Source

SPI = MSB 0 0 0 1 0 LSB

LCD_05 and 06 bias low
LCD_RS biased high
LCD_RS low = use OTP
See: EVK schematic, Page 15

F3 is EVK ETH_RESET#
F5, F6 are EVK USB_PWR_EN
E1 is EVK Eth_PWR_EN
C7 and D8 = EVK I2C
J5 is EVK USB_0_ID
K8 is EVK LCD PWM
K7 and L7 are EVK console

E10 is EVK SD1_PWR_EN

E9 is SD0 PWR_EN on both EVK and Green schematics

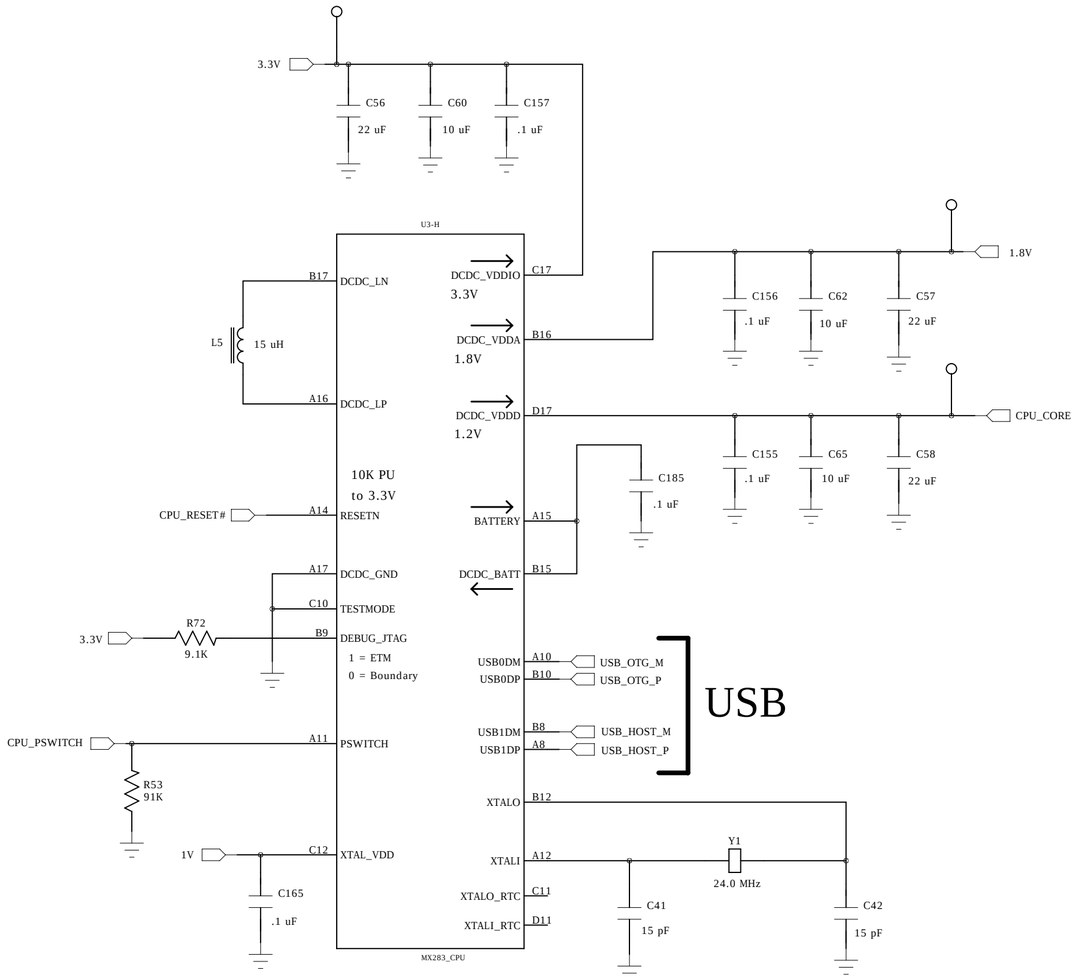
PWM outputs can be 24 MHz
divided by 16-bit integer
Allows clock 12MHz and lower

Rev.A Problems:

- Ethernet LEDs wrong !
- No CAN connected
- No A/D connected
- Add WiFi !
- Add low power modes ?
  - Pwr switch to PHY ?
- Remove FPGA ?

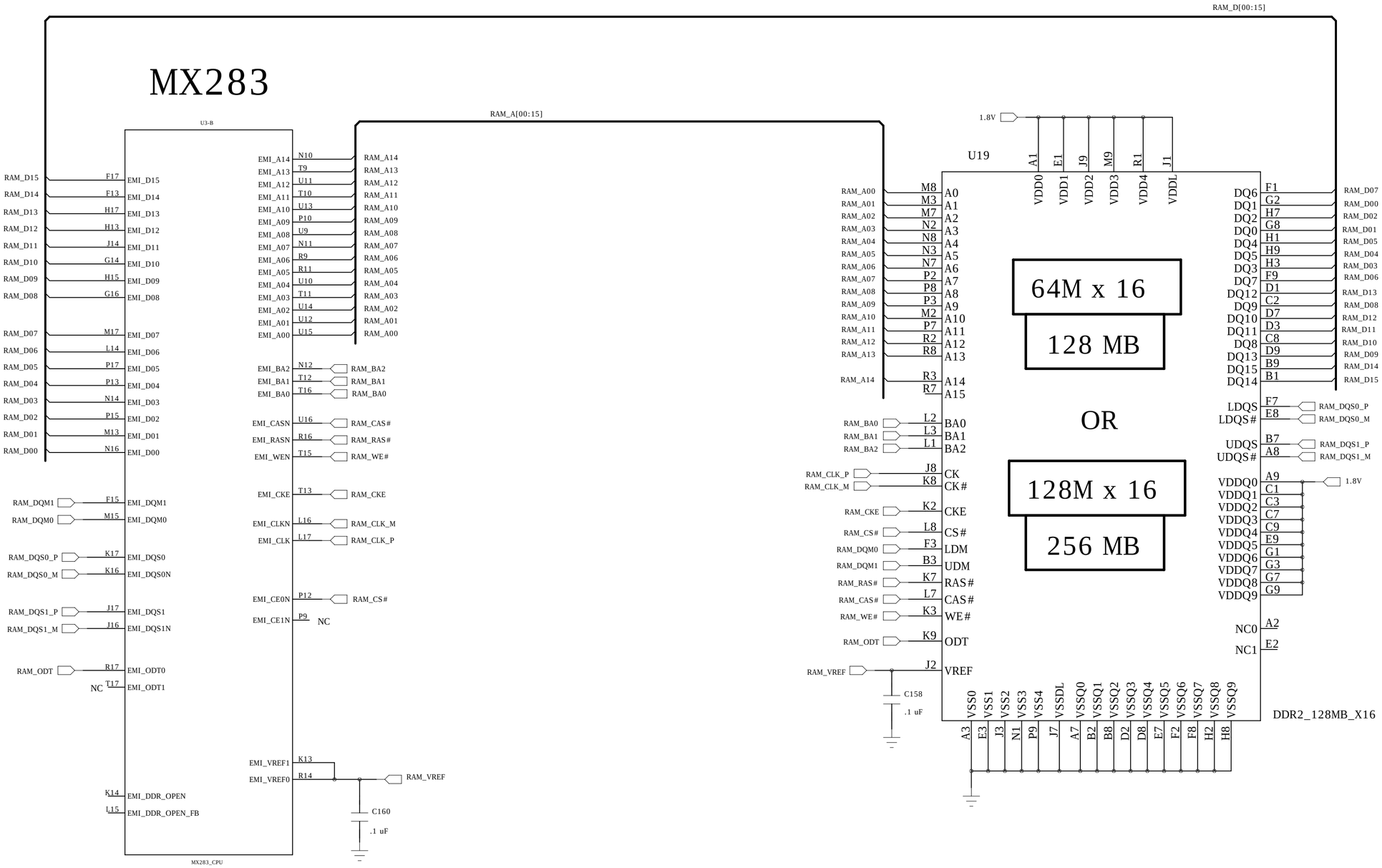
Technologic Systems	Date Feb. 21, 2014	
Title: TS-4600 MX283 CPU		
Rev: A	Designer	Sheet 1 of 9

CPU Power



Technologic Systems	Date Feb. 21, 2014	
Title: TS-4600 MX283 CPU Power		
Rev: A	Designer	Sheet 2 of 9

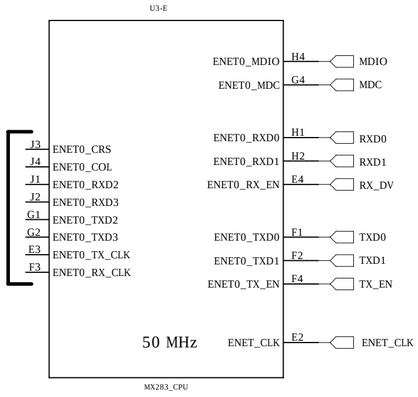
DDR2 SDRAM (128 or 256 MByte)



Technologic Systems	Date Feb. 21, 2014	
Title: TS-4600 DDR2 RAM		
Rev: A	Designer	Sheet 3 of 9

10/100 Ethernet 4-Port Switch

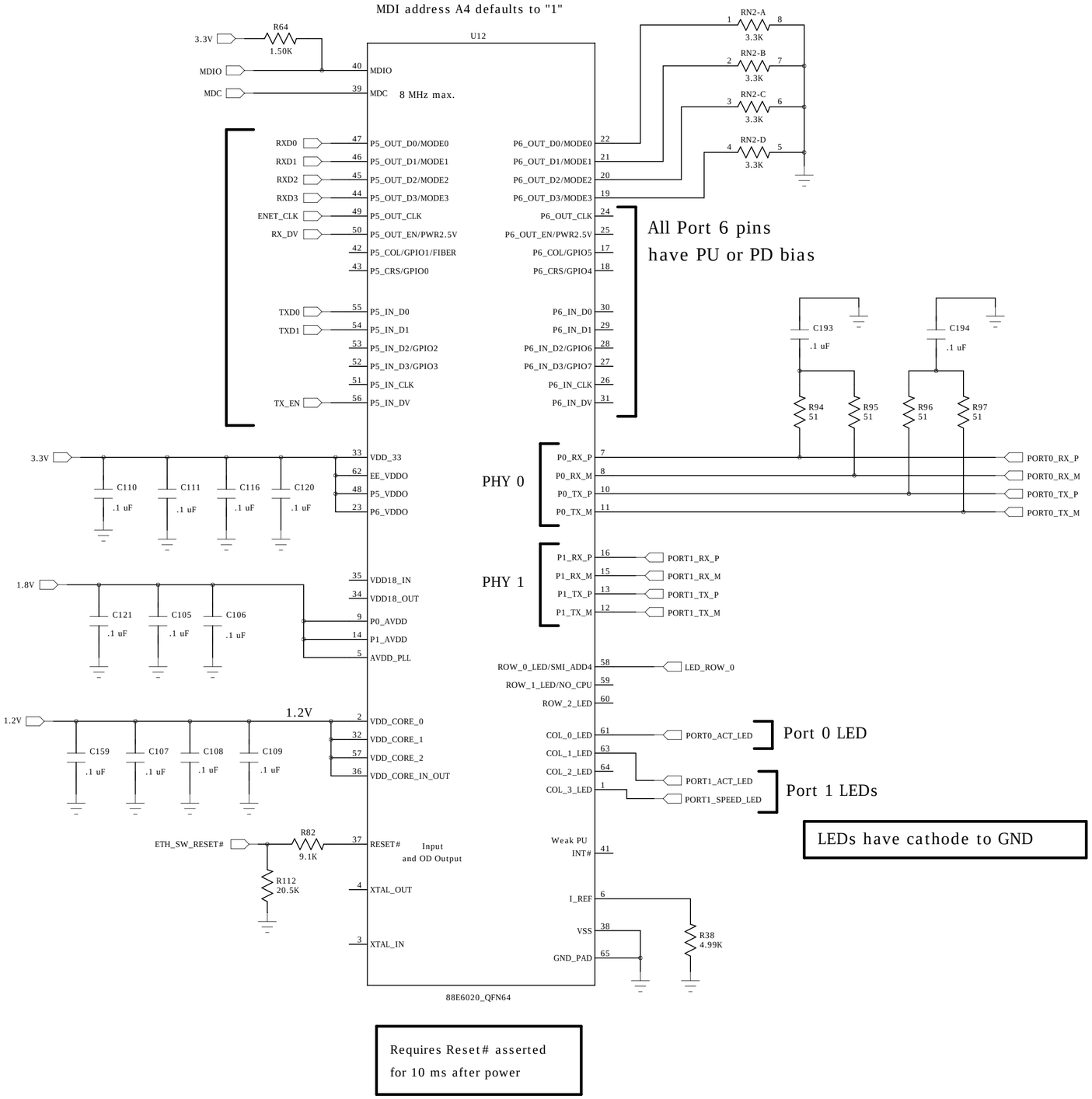
MX283



NC on MX283

Page 883 - bit 18 controls ENET_CLK direction

MDI address A4 defaults to "1"



LEDs have cathode to GND

Requires Reset# asserted for 10 ms after power

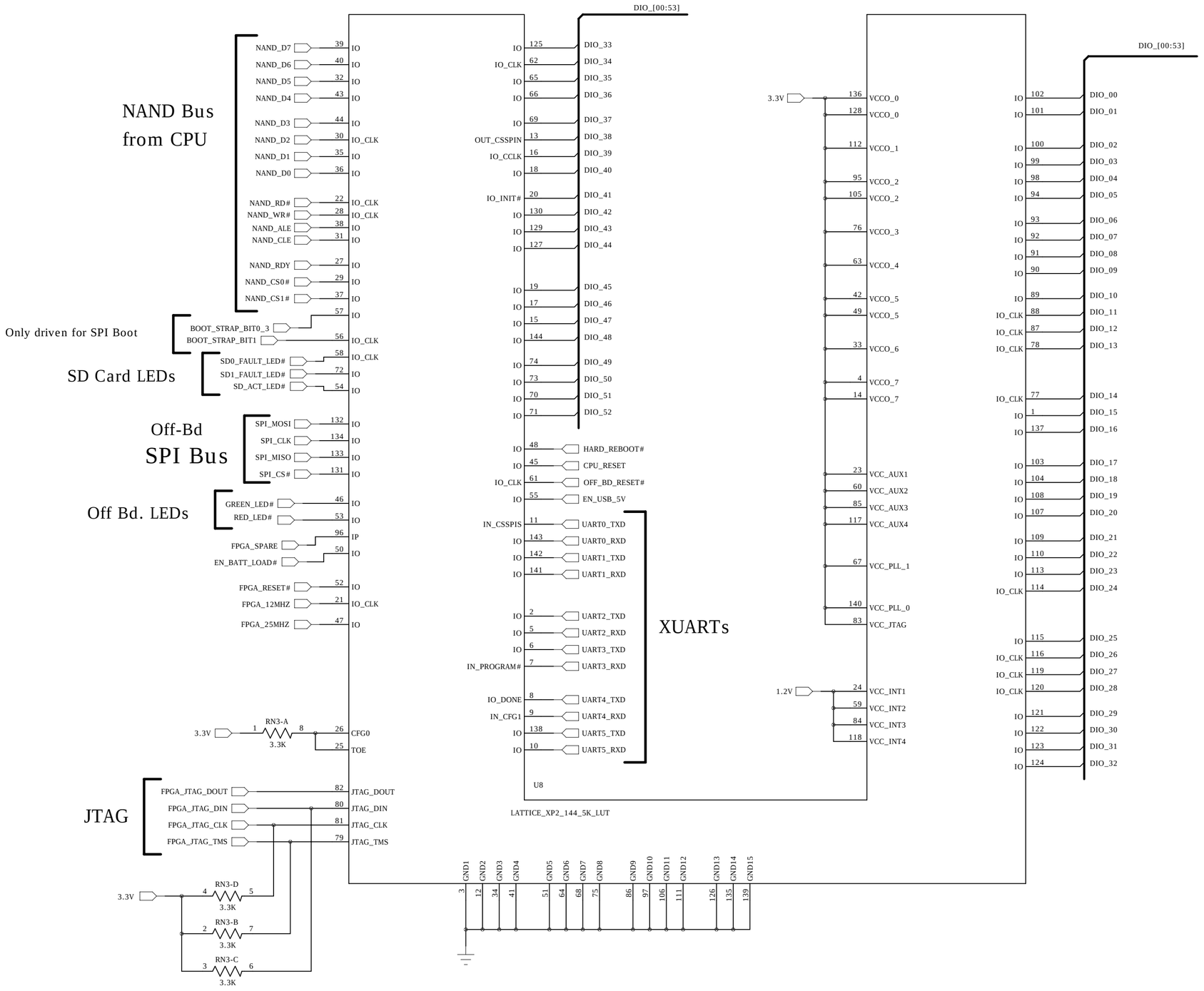
Total 88E6020 100 Mbit
Current Drain includes 2 Ports with Mag CT 3.3V Rail = 20 mA 1.8V Rail = 80 mA 1.2V Rail = 62 mA
Power Down mode 42 mA on 1.2V rail 0 mA on other rails

Auto MDIX is supported

Polarity Correction also supported

Technologic Systems		Date Feb. 21, 2014
Title: TS-4600 Ethernet Switch		
Rev: A	Designer	Sheet 4 of 9

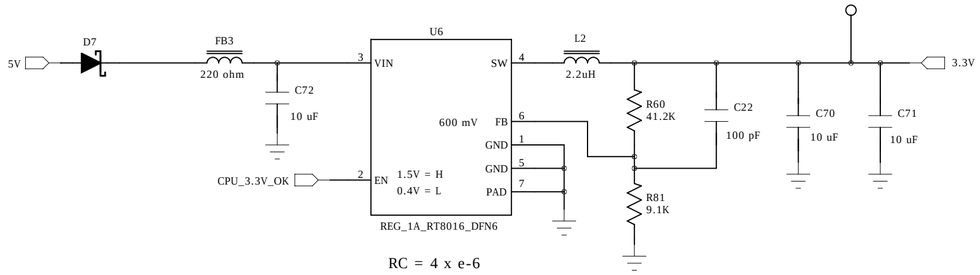
FPGA with 5K LUTs



DIO_09 is sometimes a Push switch input

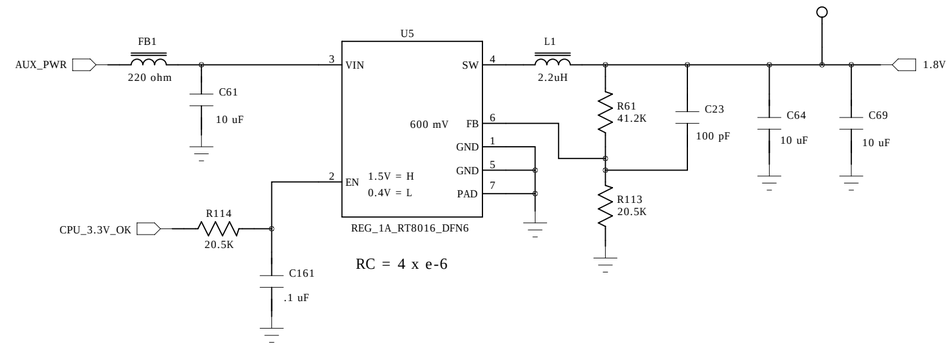
Technologic Systems	Date Feb. 21, 2014	
Title: TS-4600 FPGA		
Rev: A	Designer	Sheet 5 of 9

3.3V Reg



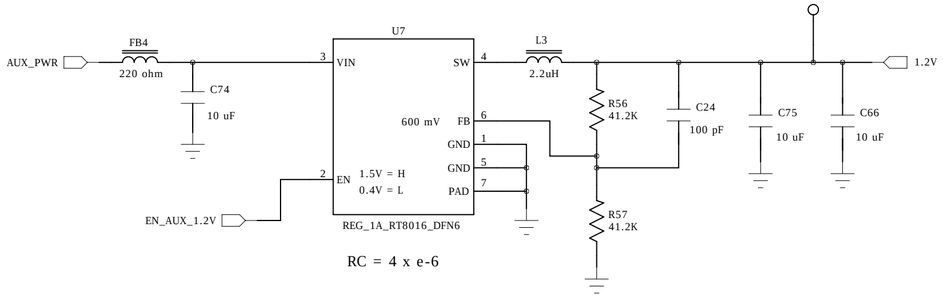
RC = 4 x e-6

1.8V Reg



RC = 4 x e-6

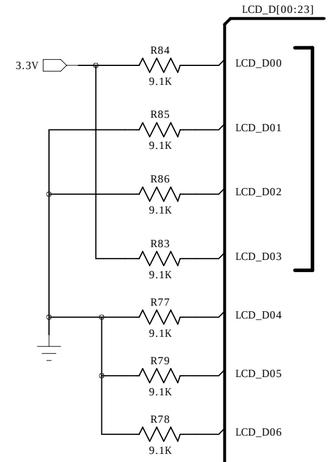
1.2V Reg.



RC = 4 x e-6

Boot Strap Bias Res.

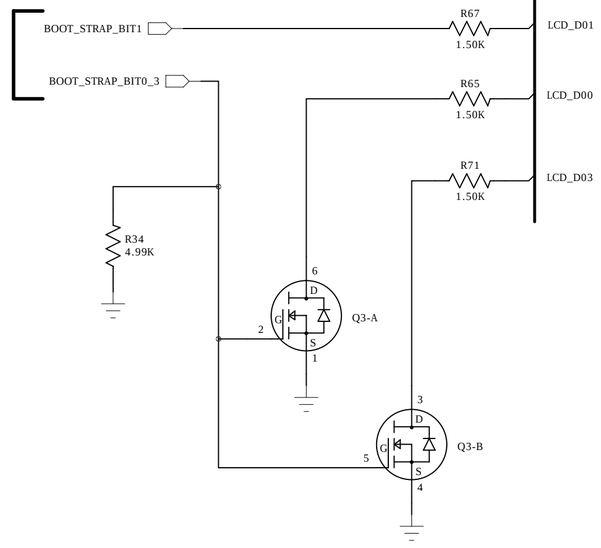
Defaults to SD Card



Boot Source

MSB			LSB	
0	0	1	0	SPI
1	0	0	1	SD Card
0	0	0	0	USB

FPGA can force SPI Flash Boot or USB Boot

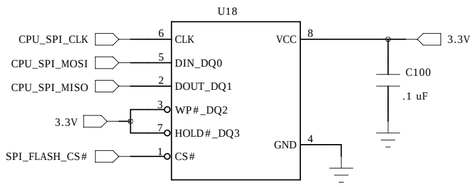


GND Test Point

Technologic Systems	Date Feb. 21, 2014	
Title: TS-4600 Power Reg. and Boot Straps		
Rev: A	Designer	Sheet 6 of 9

MX283 SPI Boot and FPGA Config Flash

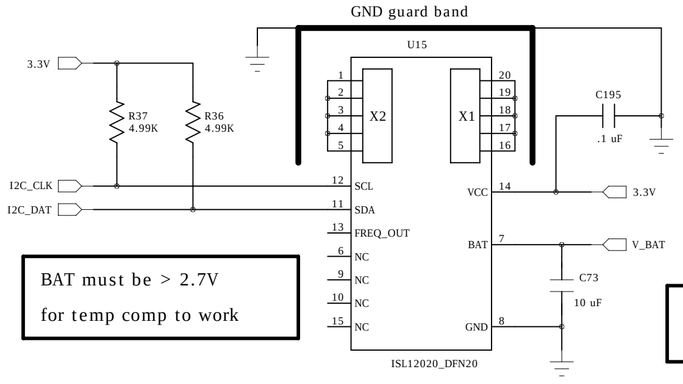
SPI Boot Flash



64 bytes of OTP

Not Populated ?

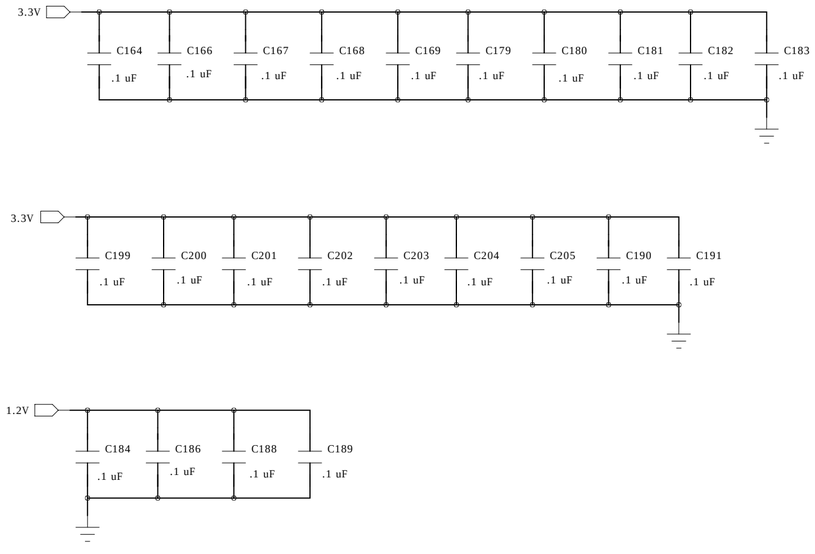
RTC and Temp. Sensor



BAT must be > 2.7V
for temp comp to work

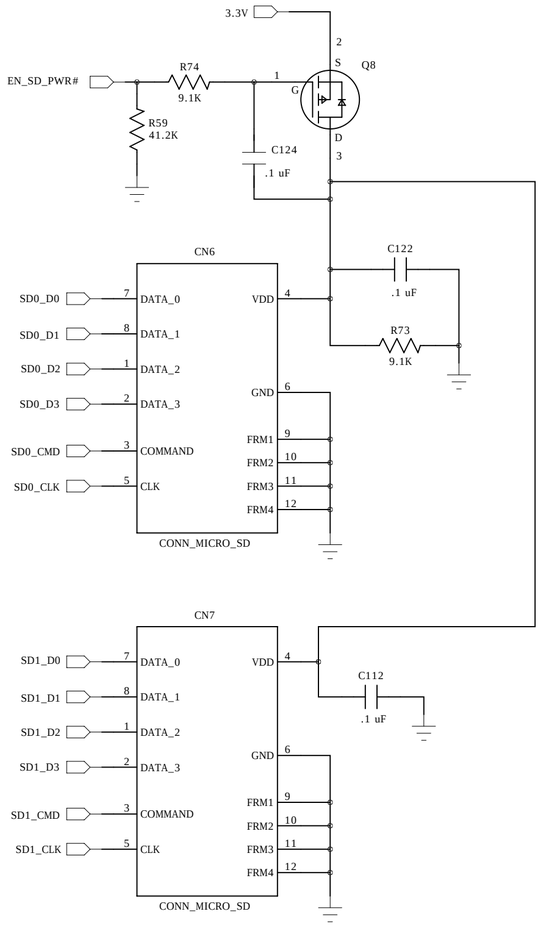
Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

FPGA Bypass Caps

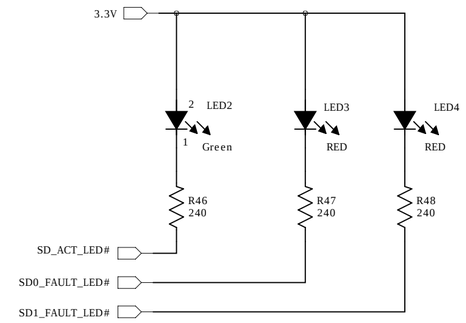


Technologic Systems		Date Feb. 21, 2014
Title: TS-4600 Boot Flash, FPGA Flash, RTC		
Rev: A	Designer	Sheet 7 of 9

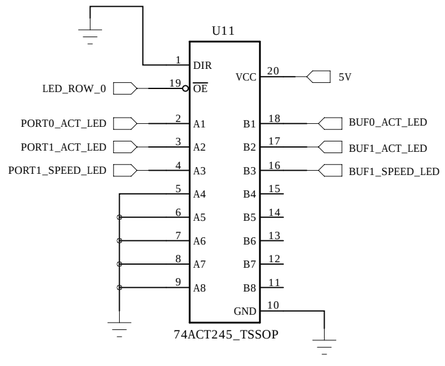
Micro SD Card Sockets



SD LEDs



Ethernet LED Buffer



Technologic Systems		Date Feb. 21, 2014
Title: TS-4600 SD Card		
Rev: A	Designer	Sheet 8 of 9

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 200 mA

REBOOT# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS (1), FPGA_JTAG_CLK (3), FPGA_JTAG_DOUT (5), FPGA_JTAG_DIN (7)

OFF_BD_RESET# is an Output
used to reset all peripherals

OFF_BD_RESET# (9), NC (11), NC (13), 5V (15), NC (17)

LCD_D08 (19), LCD_D09 (21), LCD_D10 (23), LCD_D11 (25), LCD_D12 (27), 5V (29), LCD_D13 (31), LCD_D14 (33), LCD_D15 (35), LCD_D16 (37), LCD_D17 (39), LCD_D18 (41), LCD_D19 (43), LCD_D20 (45), 5V (47), LCD_PIX_CLK (49), LCD_HSYNC (51), LCD_VSYNC (53), LCD_DE (55), LCD_PWM (57)

5V — C102 .1 uF — C101 .1 uF

DIO_[00:53]

FPGA DIO: DIO_50 (59), DIO_49 (61), DIO_14 (63), DIO_13 (65), DIO_12 (67), DIO_11 (69), DIO_10 (71), DIO_09 (73), DIO_08 (75), DIO_07 (77), DIO_06 (79), DIO_05 (81), DIO_04 (83), DIO_03 (85), DIO_02 (87), DIO_01 (89), DIO_00 (91), (93), DIO_17 (95), DIO_18 (97), (99)

HARD_REBOOT# (2), EN_USB_5V (4)

Off-Bd SD Card: SD1_D2 (6), SD1_D3 (8), SD1_CMD (10), SD_POWER (12), SD1_CLK (14), 5V (16), SD1_D0 (18), SD1_D1 (20)

LCD_D00 (22), LCD_D01 (24), LCD_D02 (26), LCD_D03 (28), LCD_D04 (30), LCD_D05 (32), V_BAT (34), LCD_D06 (36), LCD_D07 (38), LCD_D21 (40), LCD_D22 (42), LCD_D23 (44), EN_LCD_POWER (46), (48), LITH_BATT (50), (52)

16 bit Data Bus or DIO: DIO_52 (54), DIO_51 (56), DIO_37 (58), DIO_36 (60), DIO_35 (62), DIO_34 (64), DIO_33 (66), DIO_32 (68), DIO_31 (70), DIO_30 (72), DIO_29 (74), DIO_28 (76), DIO_27 (78), DIO_26 (80), DIO_25 (82), DIO_24 (84), DIO_23 (86), DIO_22 (88), DIO_21 (90), DIO_20 (92), DIO_19 (94)

DIO_[00:53]

CONN_TYCO_100PIN_SBC

Right

CN2

Primary Ethernet: PORT1_RX_P (1), PORT1_RX_M (3), 1.8V (5), PORT1_TX_P (7), PORT1_TX_M (9), 1.8V (11)

3.3V rail can supply up
to 400 mA to base board

3.3V — C196 .1 uF

USB Ports: NC (13), NC (15), NC (17), USB_HOST_M (19), USB_HOST_P (21), CPU_CORE (23), USB_OTG_M (25), USB_OTG_P (27)

1.8V (29)

SPI or DIO: SPI_CS# (31), SPI_MOSI (33), SPI_MISO (35), SPI_CLK (37)

CPU JTAG: 3.3V (39)

1V (41), CPU_PSWITCH (43)

Console: DEBUG_TXD (45), DEBUG_RXD (47), DIO_15 (49), DIO_16 (51)

BUF1_ACT_LED (2), BUF1_SPEED_LED (4), RED_LED# (6), GREEN_LED# (8), (10), BUF0_ACT_LED (12), (14)

2nd Ethernet Port: PORT0_RX_P (16), PORT0_RX_M (18), 1.8V (20), PORT0_TX_P (22), PORT0_TX_M (24), (26)

I2C: I2C_CLK (28), I2C_DAT (30)

DIO_[00:53]

DIO_48 (32)

I2S or DIO: SYS_MCLK (34), AUD_CLK (36), AUD_FRM (38), AUD_TXD (40), AUD_RXD (42)

CPU JTAG: CPU_JTAG_TMS (44), CPU_JTAG_TCK (46), CPU_JTAG_TDI (48), CPU_JTAG_TDO (50), (52)

SYS_MCLK (54)

DIO_47 (56), DIO_46 (58), DIO_45 (60), DIO_44 (62), DIO_43 (64), DIO_42 (66), DIO_41 (68), DIO_40 (70), DIO_39 (72), DIO_38 (74)

USB_OTG_ID (76)

Serial Ports or DIO: UART0_TXD (78), UART0_RXD (80), UART1_TXD (82), UART1_RXD (84), UART2_TXD (86), UART2_RXD (88), UART3_TXD (90), UART3_RXD (92), UART4_TXD (94), UART4_RXD (96), UART5_TXD (98), UART5_RXD (100)

CONN_TYCO_100PIN_SBC

If Bus is not needed, all Bus
signals can be changed to DIO

Devices connected to this bus must never
drive it when BUS_CS# is deasserted

(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

Technologic Systems		Date Feb. 21, 2014
Title: TS-4600 100 pin Connectors		
Rev: A	Designer	Sheet 9 of 9