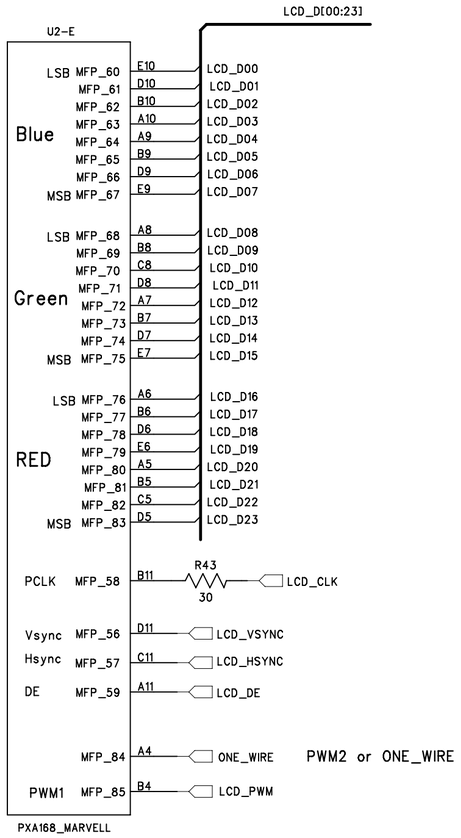
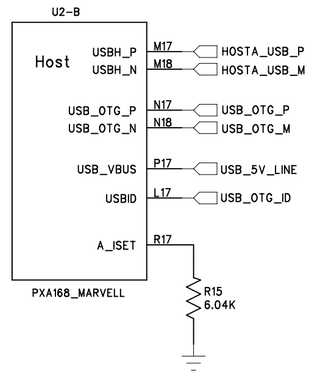
PXA166 800 MHz CPU

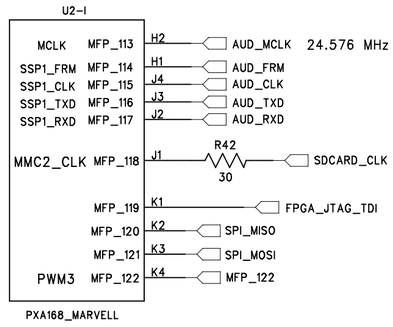
LCD



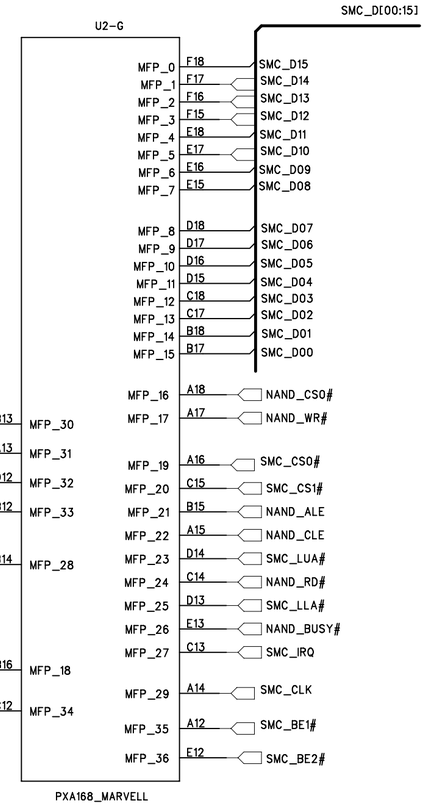
USB Ports



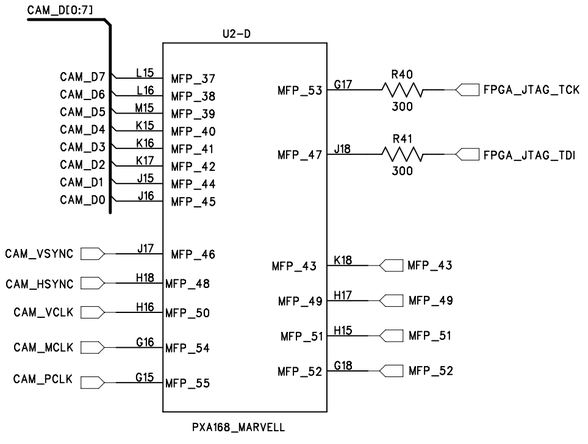
I2S



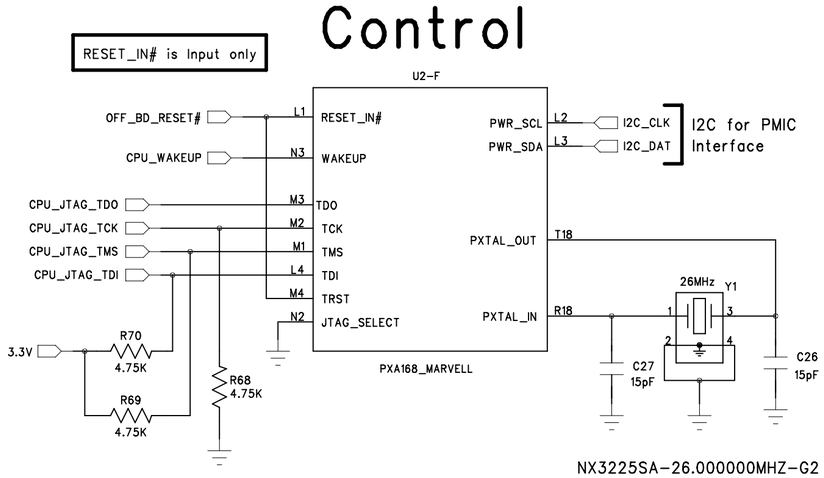
SMC Bus



Camera



Control



Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 Marvell PXA166 or PXA168		
Rev:	Designer	Sheet 1 of 8

DDR2 x8 SDRAM

256 MB

RAM_A[00:14]

CPU

U2-A

RAM_A00 R10 MA_0
RAM_A01 U10 MA_1
RAM_A02 V10 MA_2
RAM_A03 R11 MA_3
RAM_A04 U11 MA_4
RAM_A05 V11 MA_5
RAM_A06 V12 MA_6
RAM_A07 U12 MA_7
RAM_A08 T12 MA_8
RAM_A09 R12 MA_9
RAM_A10 V13 MA_10
RAM_A11 U13 MA_11
RAM_A12 R13 MA_12
RAM_A13 P13 MA_13
RAM_A14 R14 MA_14

RAM_BA0 T9 SDBA0
RAM_BA1 R9 SDBA1
RAM_BA2 P10 SDBA2

RAM_RAS# V8 SDRAS#
RAM_CAS# V9 SDCAS#
RAM_WE# U9 SDWE#
RAM_CS0# R8 SDCS0#

RAM_CKE R7 SDCKE0

RAM_CLK V6 SDCLK0
RAM_CLK# V7 SDCLK0#

RAM_LDM P1 DQM0
RAM_UDM V2 DQM1

RAM_LDQS T1 DQS0
RAM_LDQS# R1 DSQ0#

RAM_UDQS V5 DQS1
RAM_UDQS# V4 DQS1#

RAM_ODT0 U8 ODT

RAM_D[00:15]

MDQ_0 P2 RAM_D00
MDQ_1 P3 RAM_D01
MDQ_2 P4 RAM_D02
MDQ_3 R3 RAM_D03
MDQ_4 T3 RAM_D04
MDQ_5 U1 RAM_D05
MDQ_6 U2 RAM_D06
MDQ_7 V1 RAM_D07

MDQ_8 V3 RAM_D08
MDQ_9 U4 RAM_D09
MDQ_10 R5 RAM_D10
MDQ_11 T5 RAM_D11
MDQ_12 P6 RAM_D12
MDQ_13 R6 RAM_D13
MDQ_14 T6 RAM_D14
MDQ_15 U7 RAM_D15

SDCKE1 N9
SDCS1# N10
ODT1 U14
DDRESET# V14

Output

CALPAD N4
R38 300

DDR_1.8V
R80 1.0K

VREF N1
VREF
C188 .1 uF
R78 1.0K
C53 2.2uF

SEC_CS_EN N5

PXA168_MARVELL

RAM_A[00:14]

128MB x 8

U17

RAM_A00 H8 A0
RAM_A01 H3 A1
RAM_A02 H7 A2
RAM_A03 J2 A3
RAM_A04 J8 A4
RAM_A05 J3 A5
RAM_A06 J7 A6
RAM_A07 K2 A7
RAM_A08 K8 A8
RAM_A09 K3 A9
RAM_A10 H2 A10
RAM_A11 K7 A11
RAM_A12 L2 A12
RAM_A13 L8 A13
RAM_A14 L3 A14
L7 A15

RAM_BA0 G2 BA0
RAM_BA1 G3 BA1
RAM_BA2 G1 BA2

RAM_CLK E8 CK
RAM_CLK# F8 CK#

RAM_CKE F2 CKE
RAM_CS0# G8 CS#

RAM_RAS# F7 RAS#
RAM_CAS# G7 CAS#
RAM_WE# F3 WE#

RAM_ODT0 F9 ODT

VREF E2 VREF
C170 .1 uF

VDD0 A1
VDD1 E9
VDD2 H9
VDD3 L1
VDDL E1
VDDQ0 A9
VDDQ1 C1
VDDQ2 C3
VDDQ3 C7
VDDQ4 C9

DDR_1.8V

RAM_D[00:15]

DQ0 C8 RAM_D02
DQ1 C2 RAM_D06
DQ2 D7 RAM_D03
DQ6 B1 RAM_D05
DQ4 D1 RAM_D00
DQ5 D9 RAM_D04
DQ3 D3 RAM_D07
DQ7 B9 RAM_D01

DQS B7 RAM_LDQS
DQS# A8 RAM_LDQS#

DM/RDQS B3 RAM_LDM
RDQS# A2

VSS0 A3
VSS1 E3
VSS2 J1
VSS3 K9
VSSDL E7
VSSQ0 A7
VSSQ1 B2
VSSQ2 B8
VSSQ3 D2
VSSQ4 D8

RAM_DDR2_X8

RAM_A[00:14]

128MB x 8

U18

RAM_A00 H8 A0
RAM_A01 H3 A1
RAM_A02 H7 A2
RAM_A03 J2 A3
RAM_A04 J8 A4
RAM_A05 J3 A5
RAM_A06 J7 A6
RAM_A07 K2 A7
RAM_A08 K8 A8
RAM_A09 K3 A9
RAM_A10 H2 A10
RAM_A11 K7 A11
RAM_A12 L2 A12
RAM_A13 L8 A13
RAM_A14 L3 A14
L7 A15

RAM_BA0 G2 BA0
RAM_BA1 G3 BA1
RAM_BA2 G1 BA2

RAM_CLK E8 CK
RAM_CLK# F8 CK#

RAM_CKE F2 CKE
RAM_CS0# G8 CS#

RAM_RAS# F7 RAS#
RAM_CAS# G7 CAS#
RAM_WE# F3 WE#

RAM_ODT0 F9 ODT

VREF E2 VREF
C189 .1 uF

VDD0 A1
VDD1 E9
VDD2 H9
VDD3 L1
VDDL E1
VDDQ0 A9
VDDQ1 C1
VDDQ2 C3
VDDQ3 C7
VDDQ4 C9

DDR_1.8V

RAM_D[00:15]

DQ0 C8 RAM_D09
DQ1 C2 RAM_D12
DQ2 D7 RAM_D08
DQ3 D3 RAM_D14
DQ4 D1 RAM_D11
DQ5 D9 RAM_D15
DQ6 B1 RAM_D10
DQ7 B9 RAM_D13

DQS B7 RAM_UDQS
DQS# A8 RAM_UDQS#

DM/RDQS B3 RAM_UDM
RDQS# A2

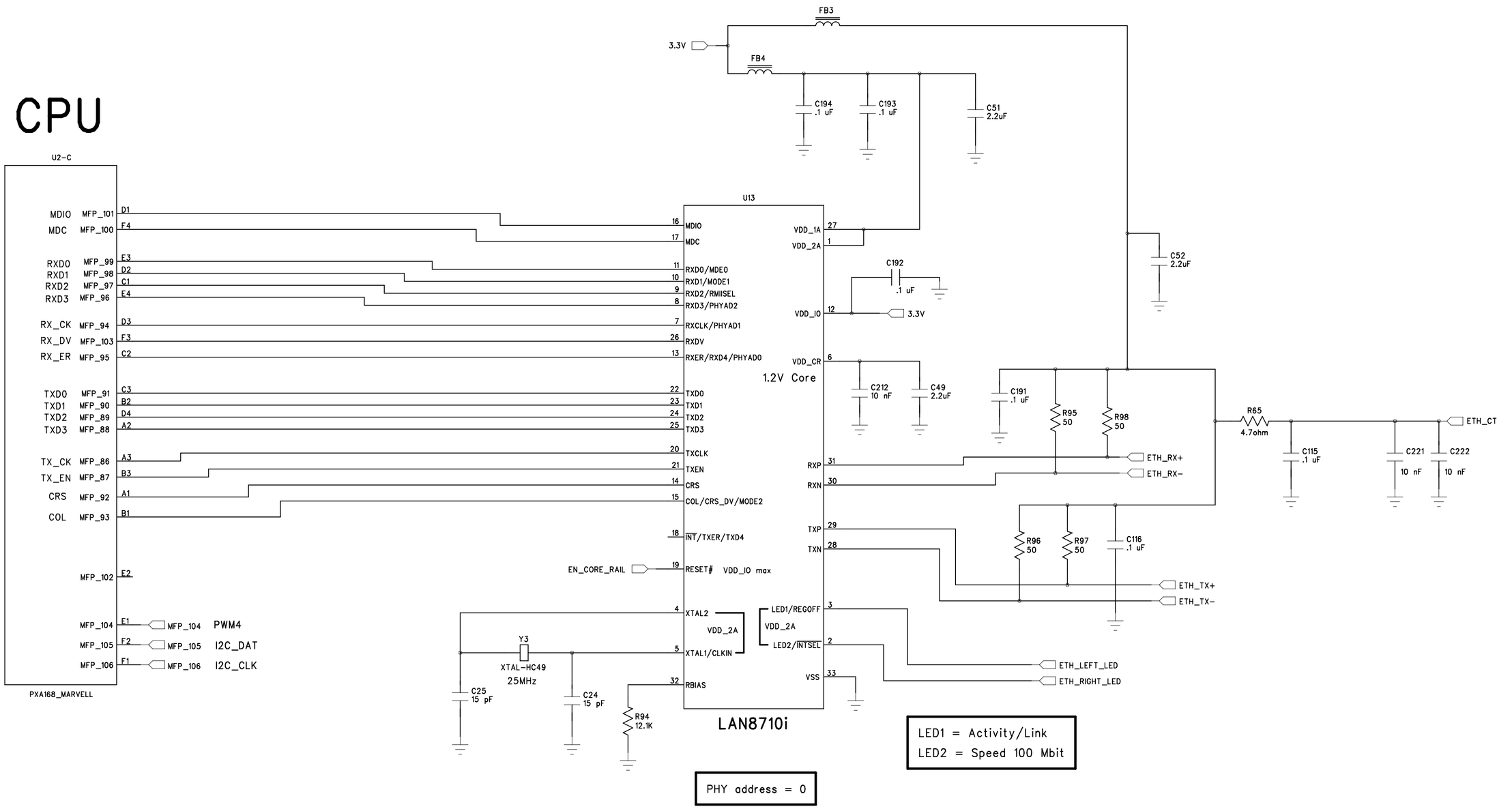
VSS0 A3
VSS1 E3
VSS2 J1
VSS3 K9
VSSDL E7
VSSQ0 A7
VSSQ1 B2
VSSQ2 B8
VSSQ3 D2
VSSQ4 D8

RAM_DDR2_X8

Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 DDR2 RAM		
Rev:	Designer	Sheet 2 of 8

10/100 Ethernet

CPU

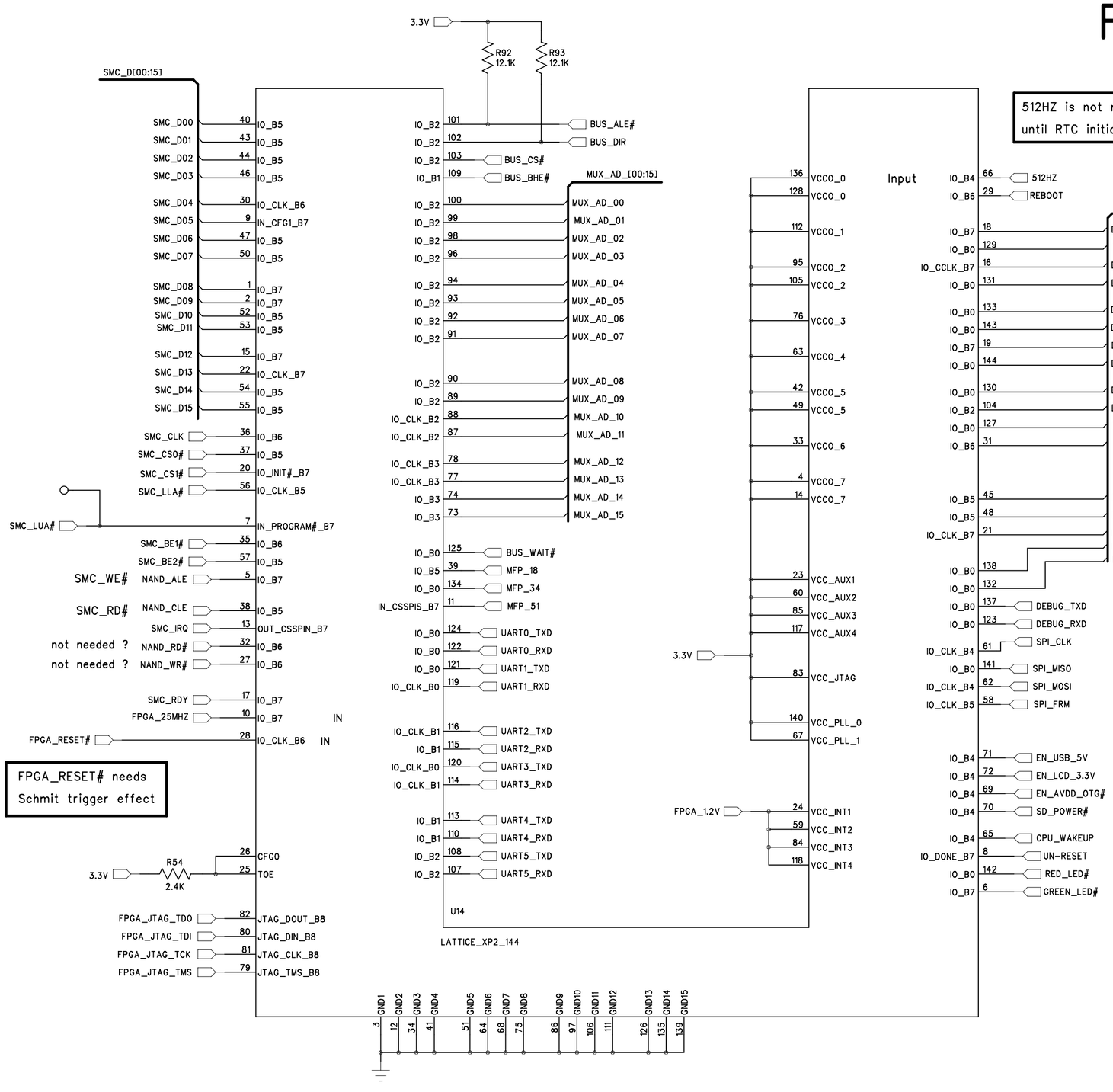


Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 Ethernet		
Rev:	Designer RLM	Sheet 3 of 8

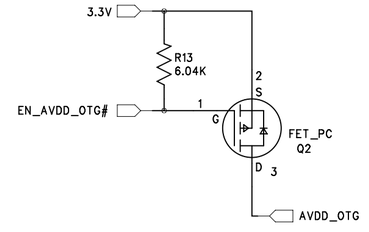
FPGA with 5000 LUTs

Boot Strap

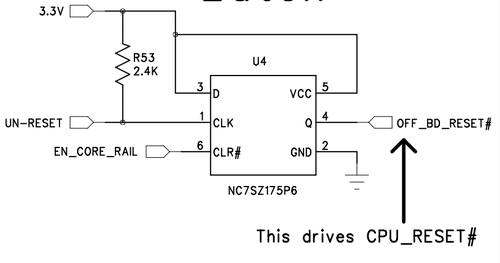
Mode 2	TS-4700 Boots from
1	NAND Flash
0	SD Card



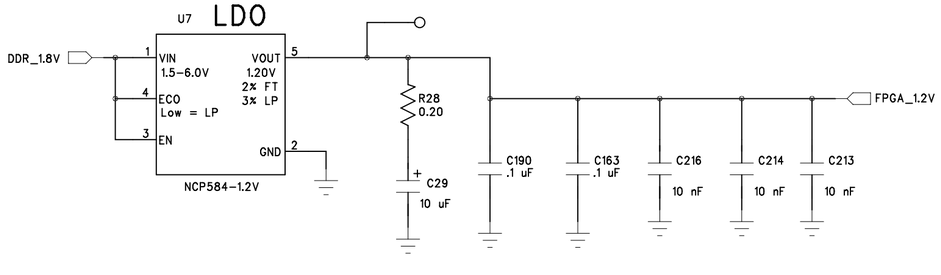
USB Power



Reset Latch



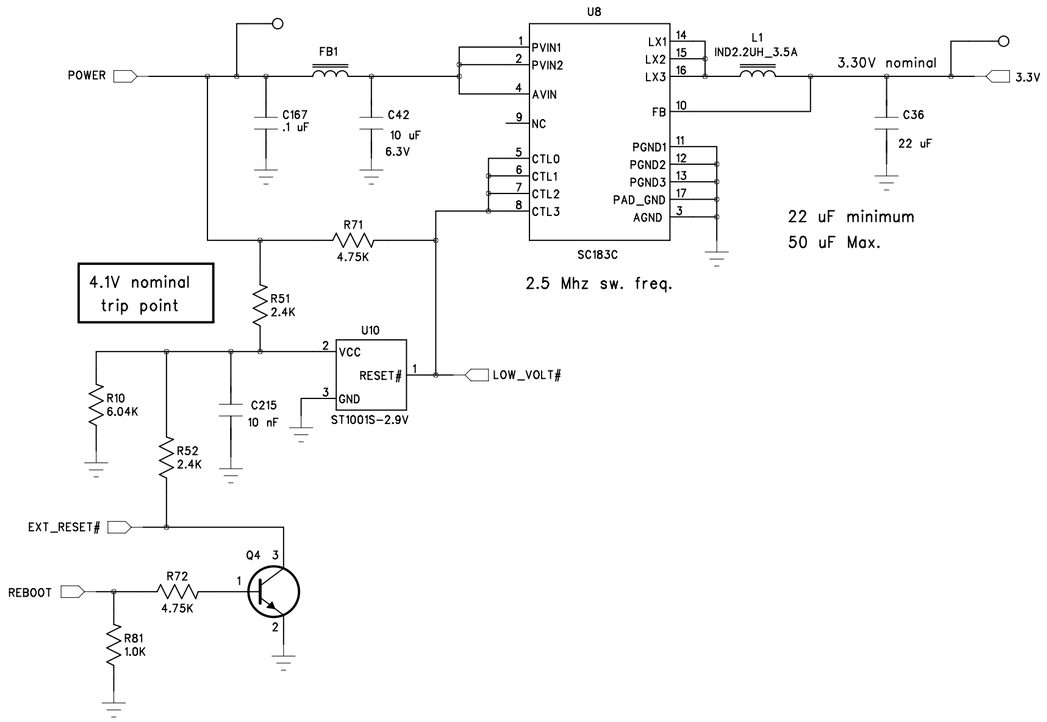
FPGA 1.2V Reg.



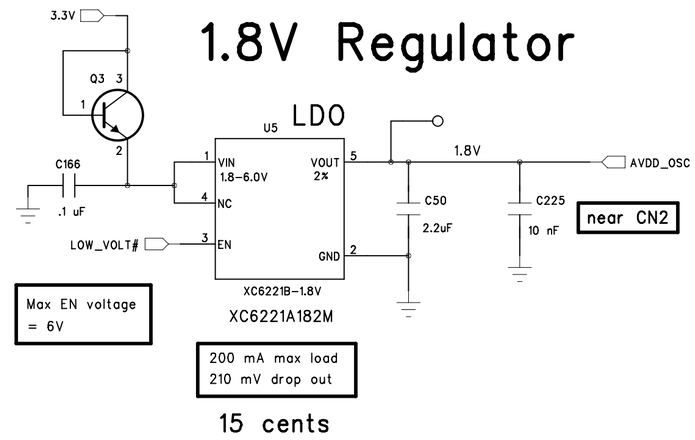
Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 FPGA		
Rev:	Designer	Sheet 4 of 8

POWER

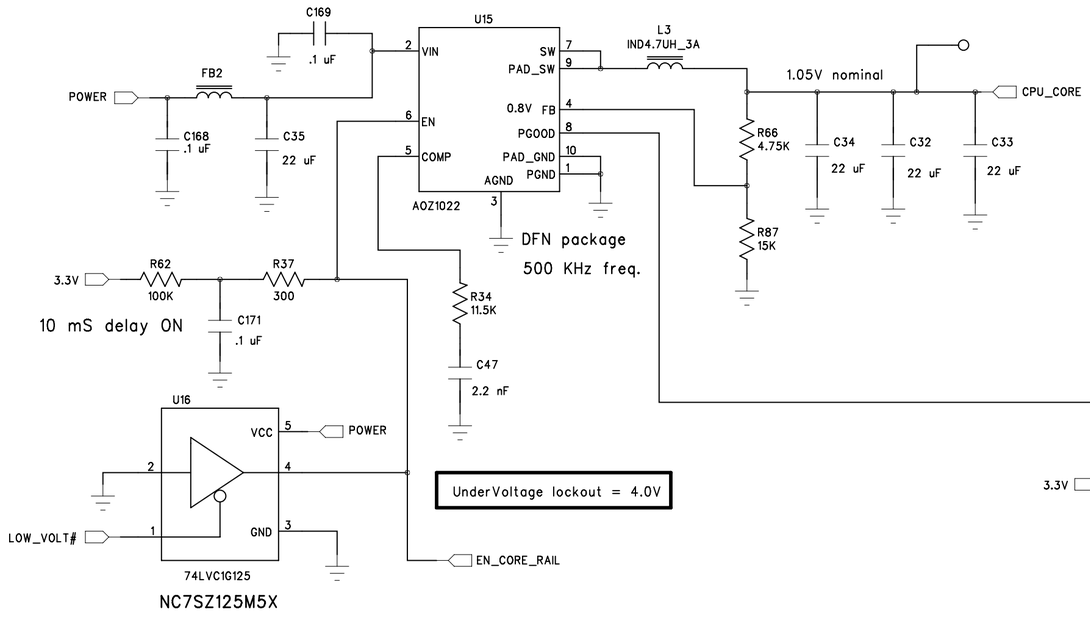
#1 3.3V Power Supply up to 2000 mA



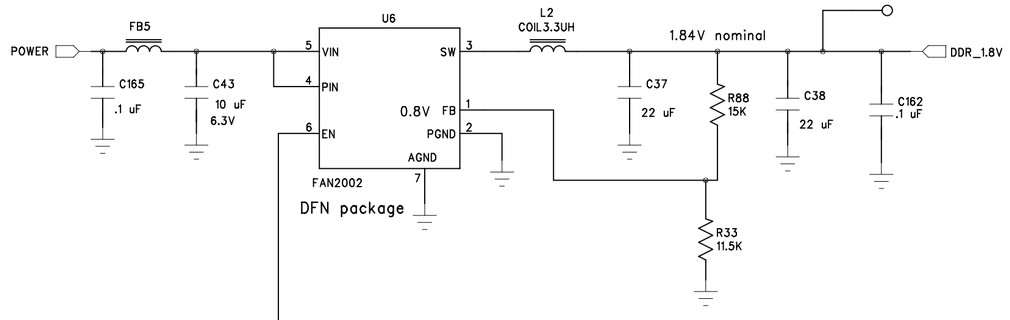
#2 1.8V Regulator



#3 CPU Core Supply

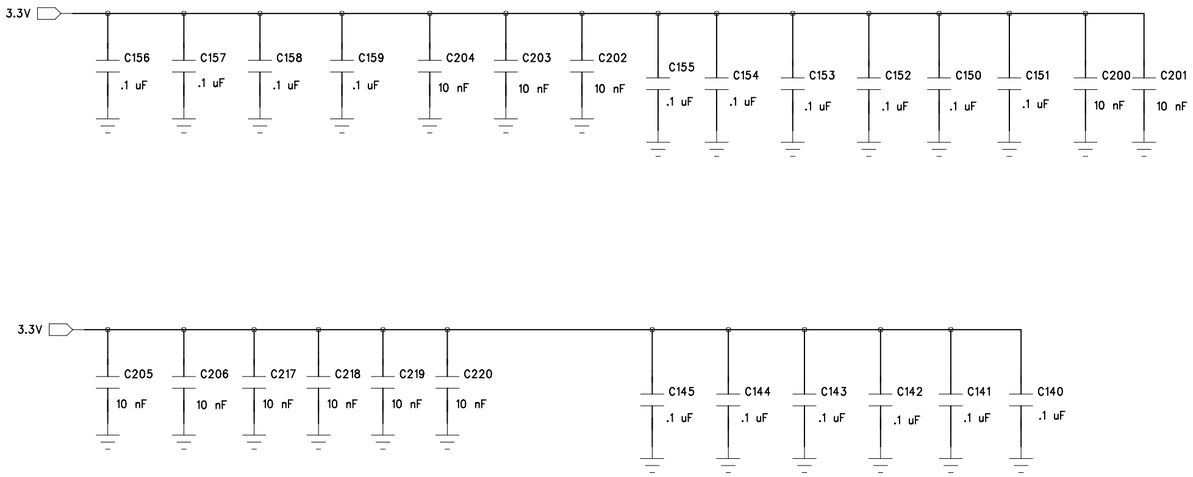


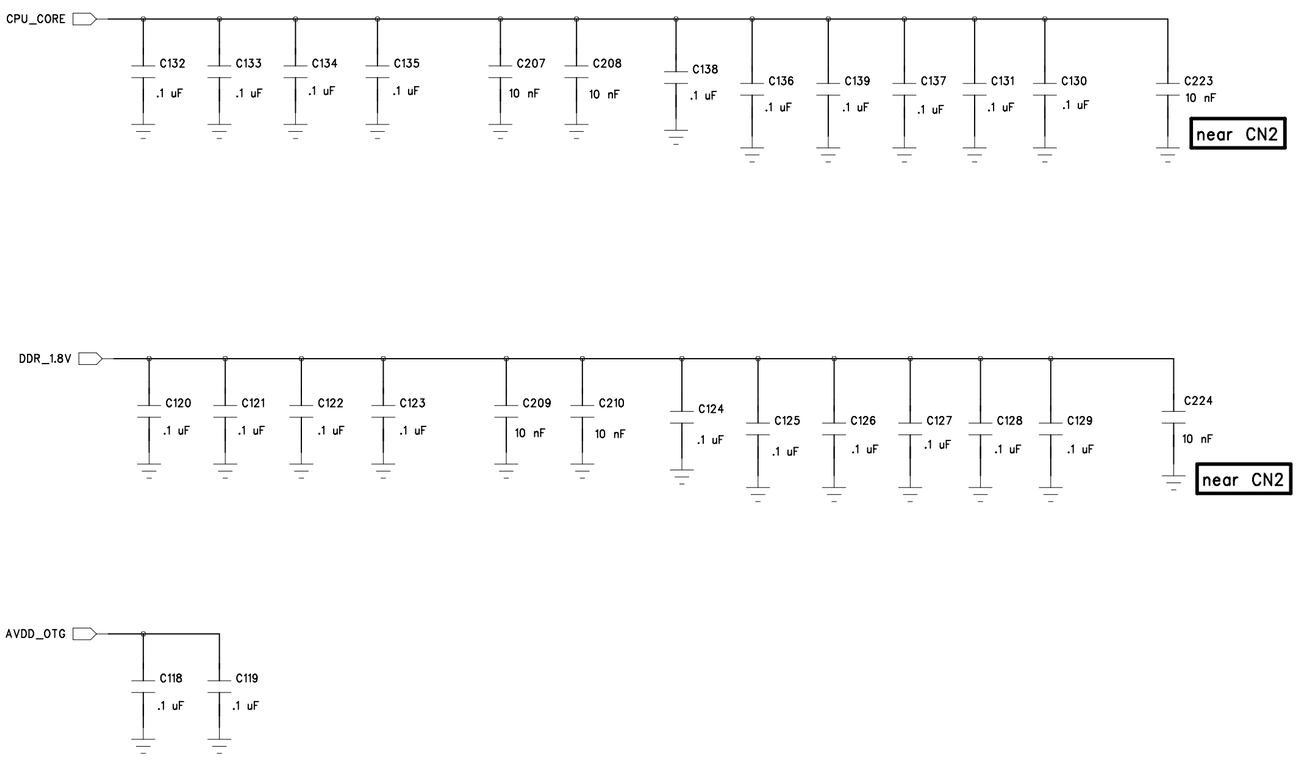
#4 DDR 1.8V Reg.



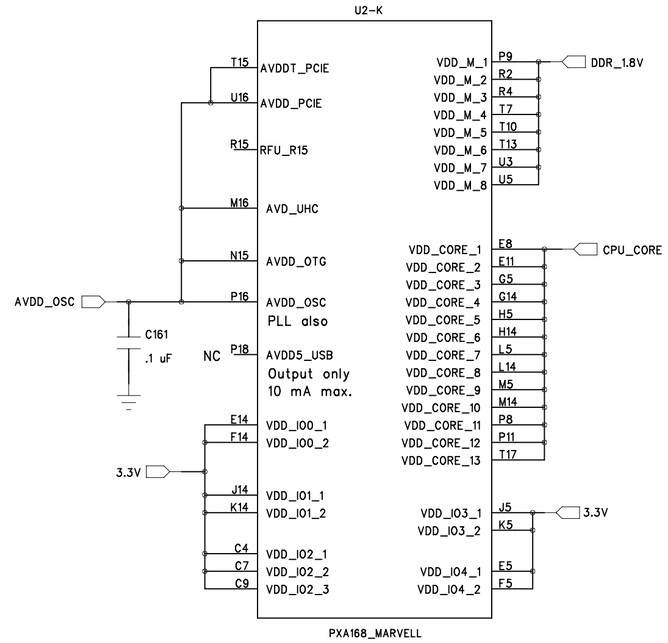
Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 Power Supplies		
Rev:	Designer	Sheet 5 of 8

CPU Power

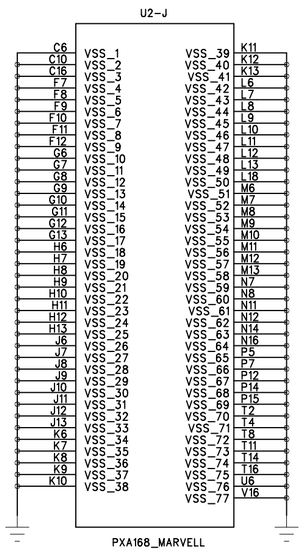




CPU

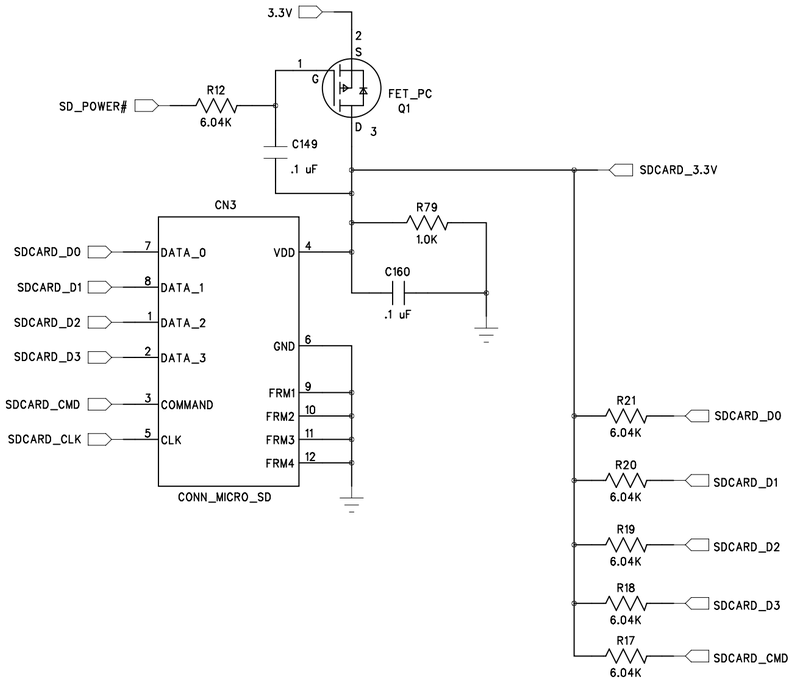


CPU

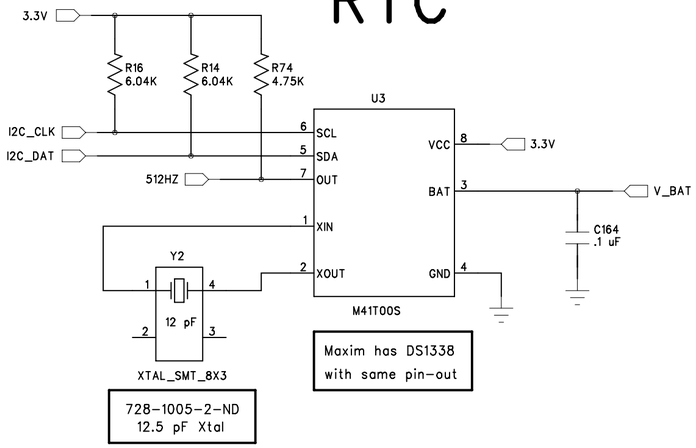


Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 CPU Power and Bypass caps		
Rev:	Designer	Sheet 6 of 8

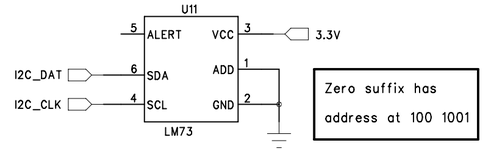
Micro SD Card Socket



RTC

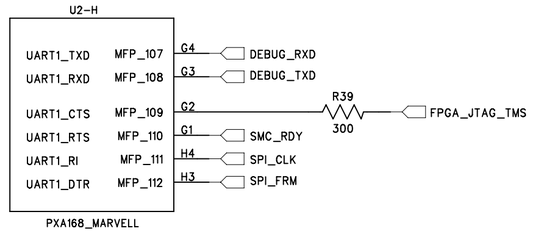


Temp Sensor



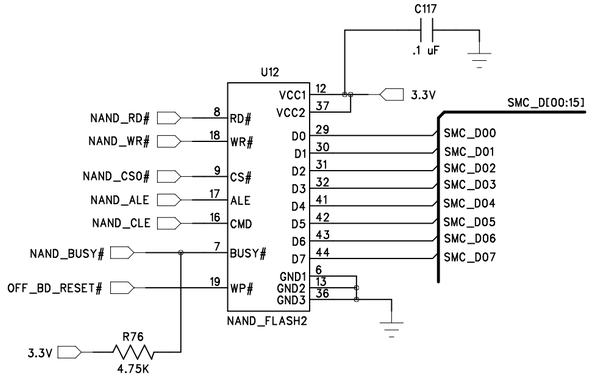
CPU

UART 1



512 Mbyte

NAND Flash



Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 SD card, NAND, RTC		
Rev:	Designer	Sheet 7 of 8

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is approximately 400 mA

EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

Left

CN1

FPGA JTAG: FPGA_JTAG_TMS 1, FPGA_JTAG_TCK 3, FPGA_JTAG_TDO 5, FPGA_JTAG_TDI 7, OFF_BD_RESET# 9

NC 11, NC 13, POWER 15, POWER_FAIL# 17, NC 19

LCD_D08 21, LCD_D09 23, LCD_D10 25, LCD_D11 27, LCD_D12 29

POWER — C146 .1 uF, C148 .1 uF

LCD_D13 31, LCD_D14 33, LCD_D15 35, LCD_D16 37, LCD_D17 39, LCD_D18 41, LCD_D19 43, LCD_D20 45

POWER 47

LCD_CLK 49, LCD_HSYNC 51, LCD_VSYNC 53, LCD_DE 55, LCD_PWM 57

59, 61

DIO_[00:16]

FPGA DIO: DIO_14 63, DIO_13 65, DIO_12 67, DIO_11 69, DIO_10 71, DIO_09 73, DIO_08 75, DIO_07 77, DIO_06 79, DIO_05 81, DIO_04 83, DIO_03 85, DIO_02 87, DIO_01 89, DIO_00 91

93, BUS_WAIT# 95, BUS_BHE# 97, 99

2 EXT_RESET#, 4 EN_USB_5V, 6 SDCARD_D2, 8 SDCARD_D3, 10 SDCARD_CMD, 12 SDCARD_3.3V, 14 SDCARD_CLK, 16 POWER, 18 SDCARD_D0, 20 SDCARD_D1

Off-Bd SD Card — uses MMC2 signals

22, 24 LCD_D00, 26 LCD_D01, 28 LCD_D02, 30 LCD_D03, 32 LCD_D04, 34 LCD_D05, 36 V_BAT, 38 LCD_D06, 40 LCD_D07, 42 LCD_D21, 44 LCD_D22, 46 LCD_D23, 48 EN_LCD_3.3V, 50, 52, 54, 56, 58, 60, 62

64 MUX_AD_15, 66 MUX_AD_14, 68 MUX_AD_13, 70 MUX_AD_12, 72 MUX_AD_11, 74 MUX_AD_10, 76 MUX_AD_09, 78 MUX_AD_08, 80 MUX_AD_07, 82 MUX_AD_06, 84 MUX_AD_05, 86 MUX_AD_04, 88 MUX_AD_03, 90 MUX_AD_02, 92 MUX_AD_01, 94 MUX_AD_00

Data Bus or DIO

96 BUS_ALE#, 98 BUS_DIR, 100 BUS_CS#

MUX_AD_[00:15]

TYCO_100PIN

Bus Control

OFF_BD_RESET# is an Output
used to reset all peripherals

Right

CN2

Ethernet: ETH_RX+ 1, ETH_RX- 3, ETH_CT 5, ETH_TX+ 7, ETH_TX- 9, ETH_CT 11, 3.3V 13

15, 17, 19, 21

NC 23, NC 25, NC 27

USB Ports: HOSTA_USB_M 29, HOSTA_USB_P 31, CPU_CORE 33, USB_OTG_M 35, USB_OTG_P 37, 3.3V 39

41, 43, 45, 47, 49, 51, 53, 55

DDR_1.8V 57

59, 61

AVDD_OSC 63

SPI or DIO: SPI_FRM 65, SPI_MOSI 67, SPI_MISO 69, SPI_CLK 71

73, 75, 77

CPU JTAG Vcc 3.3V 79

Camera or DIO: CAM_D3 81, CAM_D4 83, CAM_PCLK 85, CAM_VCLK 87, MFP_52 89, MFP_43 91

Console: DEBUG_TXD 93, DEBUG_RXD 95

CAN: DIO_15 97, DIO_16 99

2 ETH_LEFT_LED, 4 ETH_RIGHT_LED, 6 RED_LED#, 8 GREEN_LED#, 10 MFP_105, 12 MFP_106, 14 MFP_122

16, 18, 20, 22, 24

A/D

26 MFP_49, 28 I2C_CLK, 30 I2C_DAT

I2C

32 MFP_104, 34 AUD_MCLK, 36 AUD_CLK, 38 AUD_FRM, 40 AUD_TXD, 42 AUD_RXD

I2S or DIO

44 CPU_JTAG_TMS, 46 CPU_JTAG_TCK, 48 CPU_JTAG_TDI, 50 CPU_JTAG_TDO

CPU JTAG

52 ONE_WIRE, 54 MFP_51, 56 CAM_MCLK, 58 CAM_D0, 60 CAM_D1, 62 CAM_D2, 64 CAM_D5, 66 CAM_D6, 68 CAM_D7, 70 CAM_HSYNC, 72 CAM_VSYNC

Camera or DIO

74 USB_OTG_ID, 76 USB_5V_LINE

78 UART0_TXD, 80 UART0_RXD, 82 UART1_TXD, 84 UART1_RXD, 86 UART2_TXD, 88 UART2_RXD, 90 UART3_TXD, 92 UART3_RXD, 94 UART4_TXD, 96 UART4_RXD, 98 UART5_TXD, 100 UART5_RXD

Serial Ports or DIO

TYCO_100PIN

3.3V rail can supply up
to 700 mA to base board

MFP_105 and MFP_106 can be
used as a second I2C bus

MFP_122 = PWM3

MFP_104 = PWM4

CN2-54 Codec CLK
on the TS-8390

MFP_51, SPI_CLK
SPI_FRM, SPI_MOSI
and SPI_MISO
have FPGA pins
in parallel

** Can use either

DIO_15 and DIO_16
can be CAN_TXD
and CAN_RXD

Boot Strap

Mode 2	TS-4700 Boots from
1	NAND Flash
0	SD Card

BUS_DIR is latched prior to
OFF_BD_RESET# deasserted

Connect 1.5K ohm resistor
between BUS_DIR and
OFF_BD_RESET# to set low
(Boot from SD card)

BUS_DIR = MODE2

If Bus is not needed, all Bus
signals can be changed to DIO

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

Technologic Systems	Date Nov. 3, 2010	
Title: TS-4700 Off-board Connectors		
Rev:	Designer	Sheet 8 of 8