

Rev.A Notes:

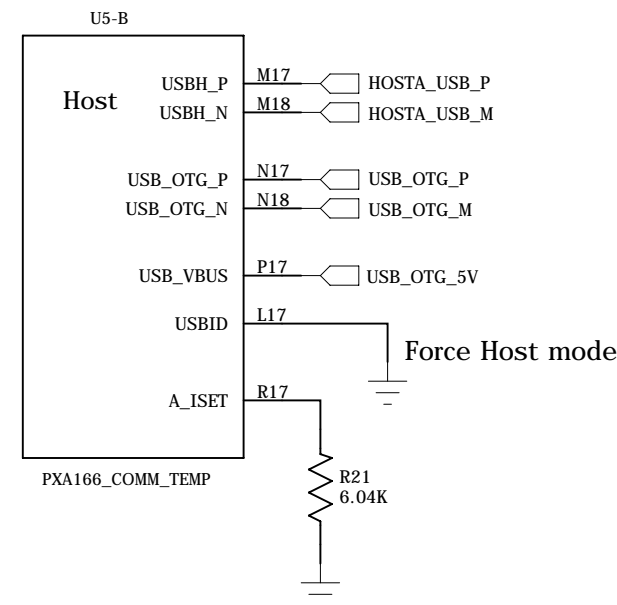
PXA166 800 MHz - PXA168 1066 MHz

- D6 and TVS6 not pop ?
- R113 pop ? (PS_MODE)
- R78 not pop for PXA166
- FB16 and FB17 not pop
- No stencil change !!

Changes from Rev.P2

- Change FB22 to 0 ohm (R69)
- Added PD on EN_SINK_1.2V
- U13 EN pin connected to 5V
- Model = TS-7250-V2 Rev.A

USB Ports

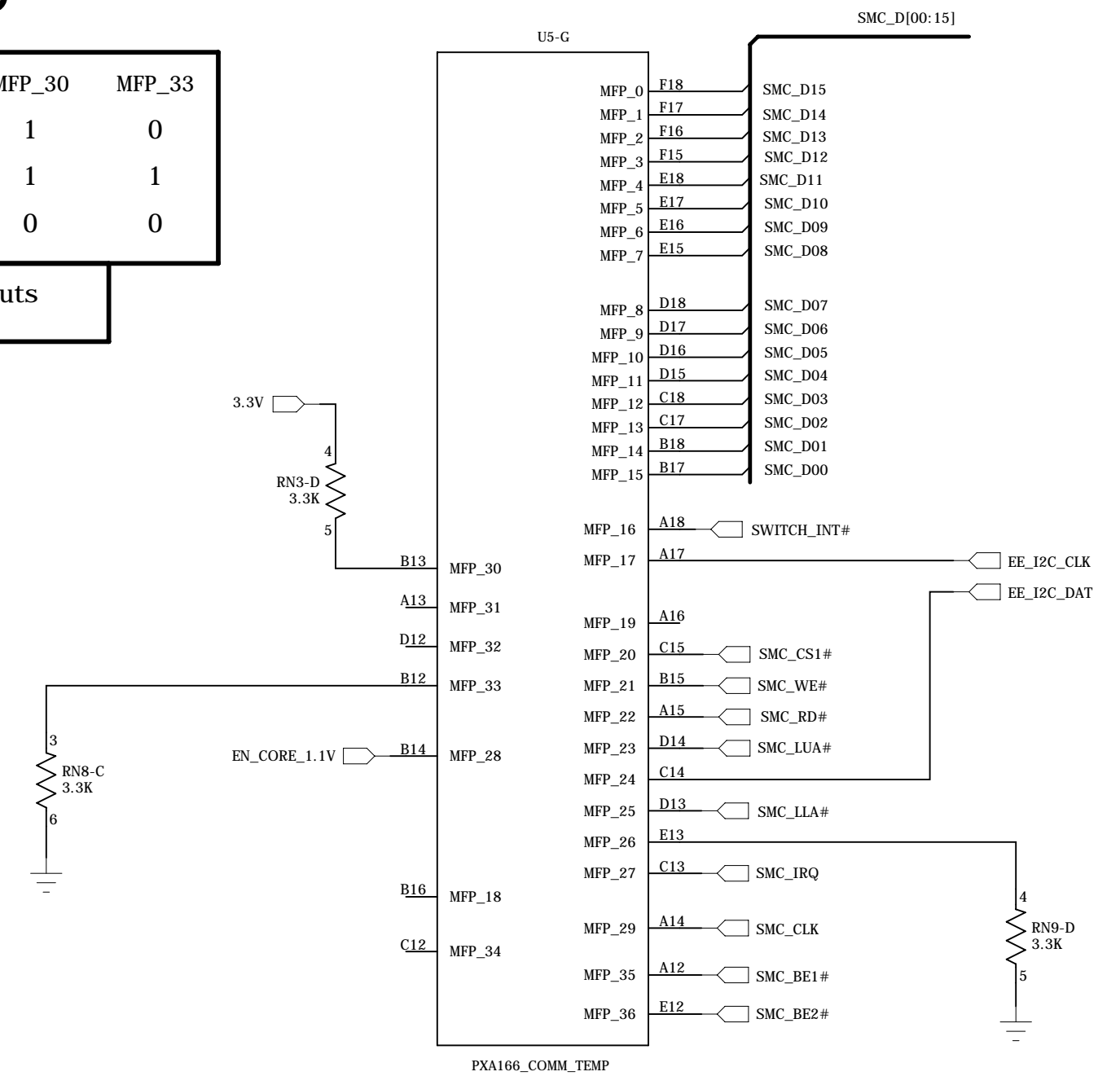


Board ID

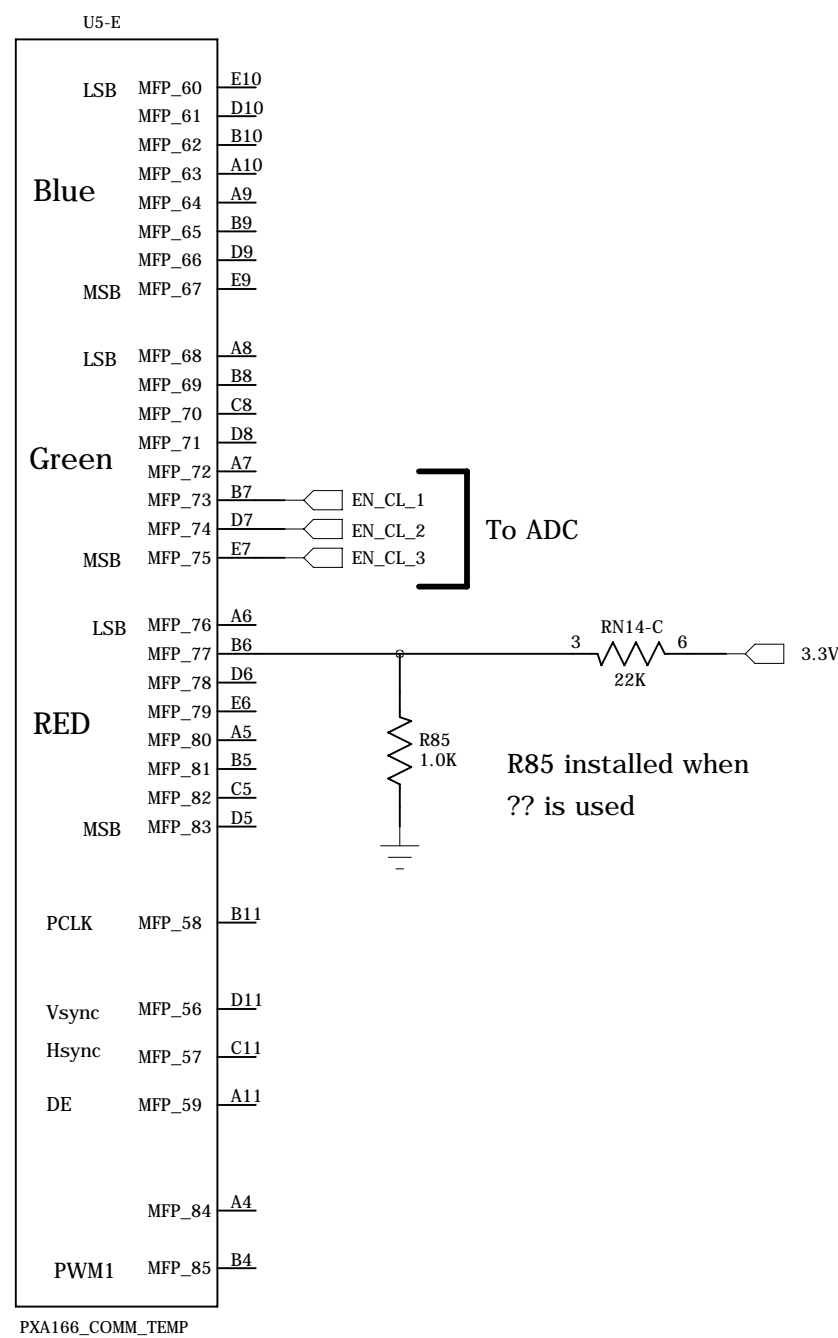
	MFP_26	MFP_30	MFP_33
TS-7250_V2	0	1	0
TS-7800_V2	1	1	1
TS-xxxx	0	0	0

Requires MFP to be Inputs

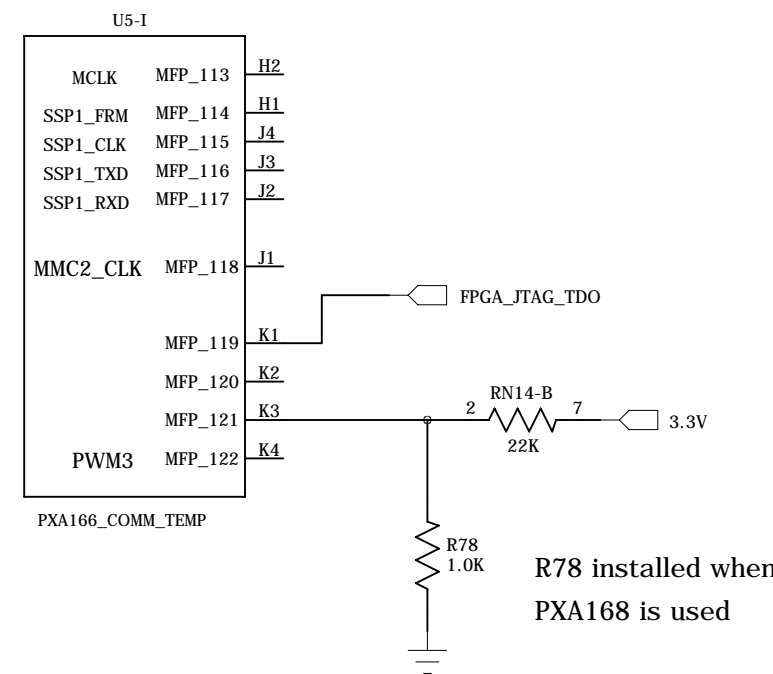
SMC Bus



LCD

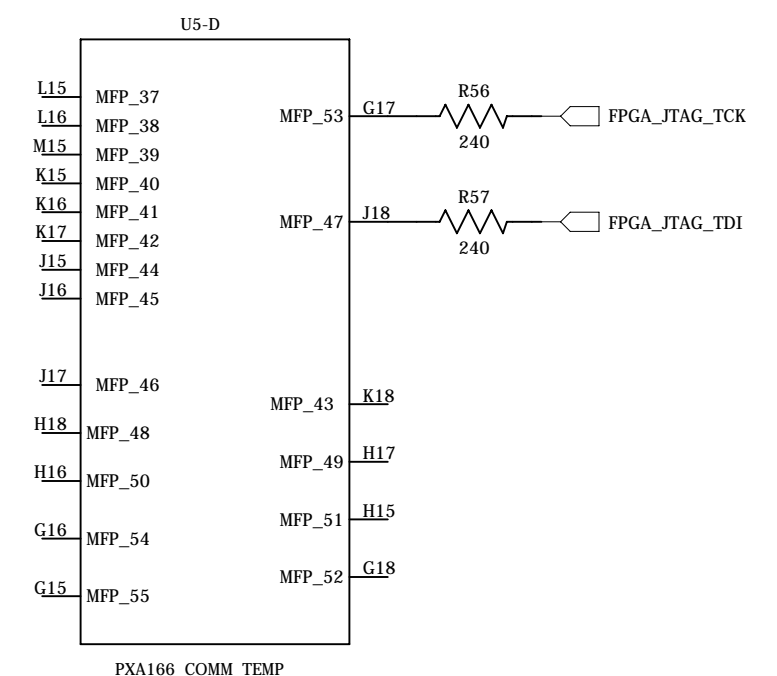


I2S

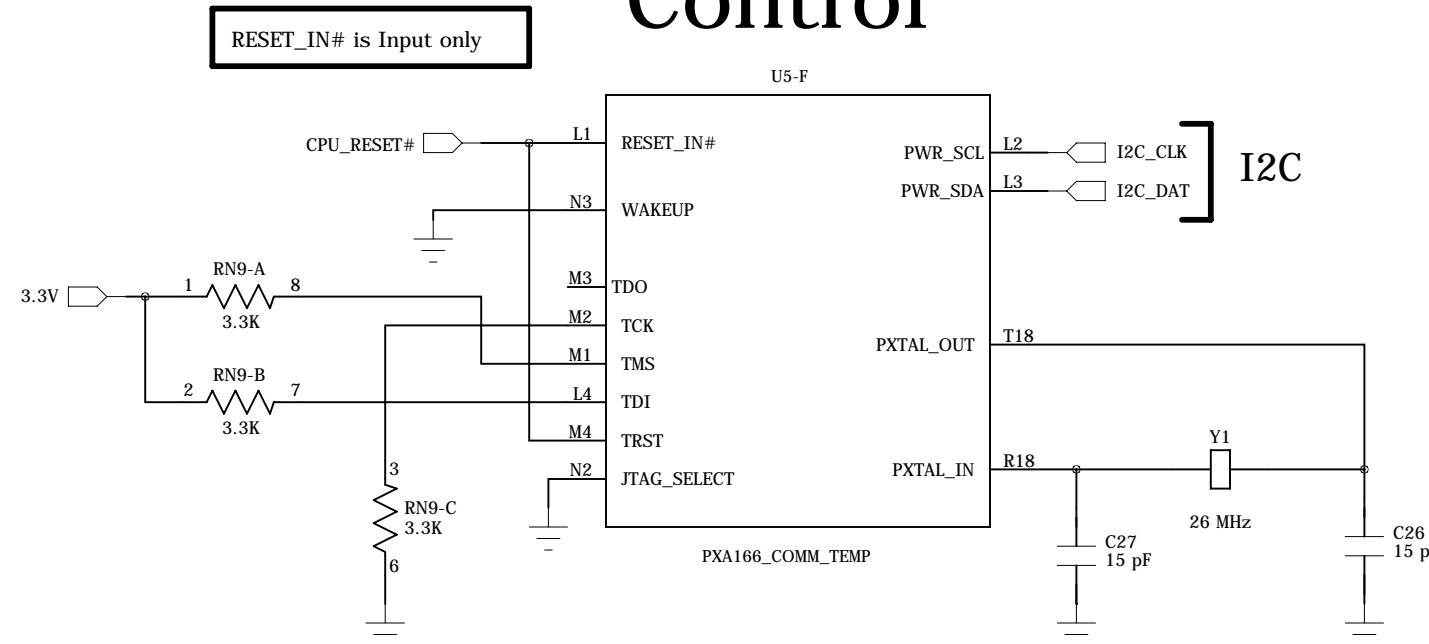


R78 installed when PXA168 is used

Camera



Control



RESET_IN# is Input only

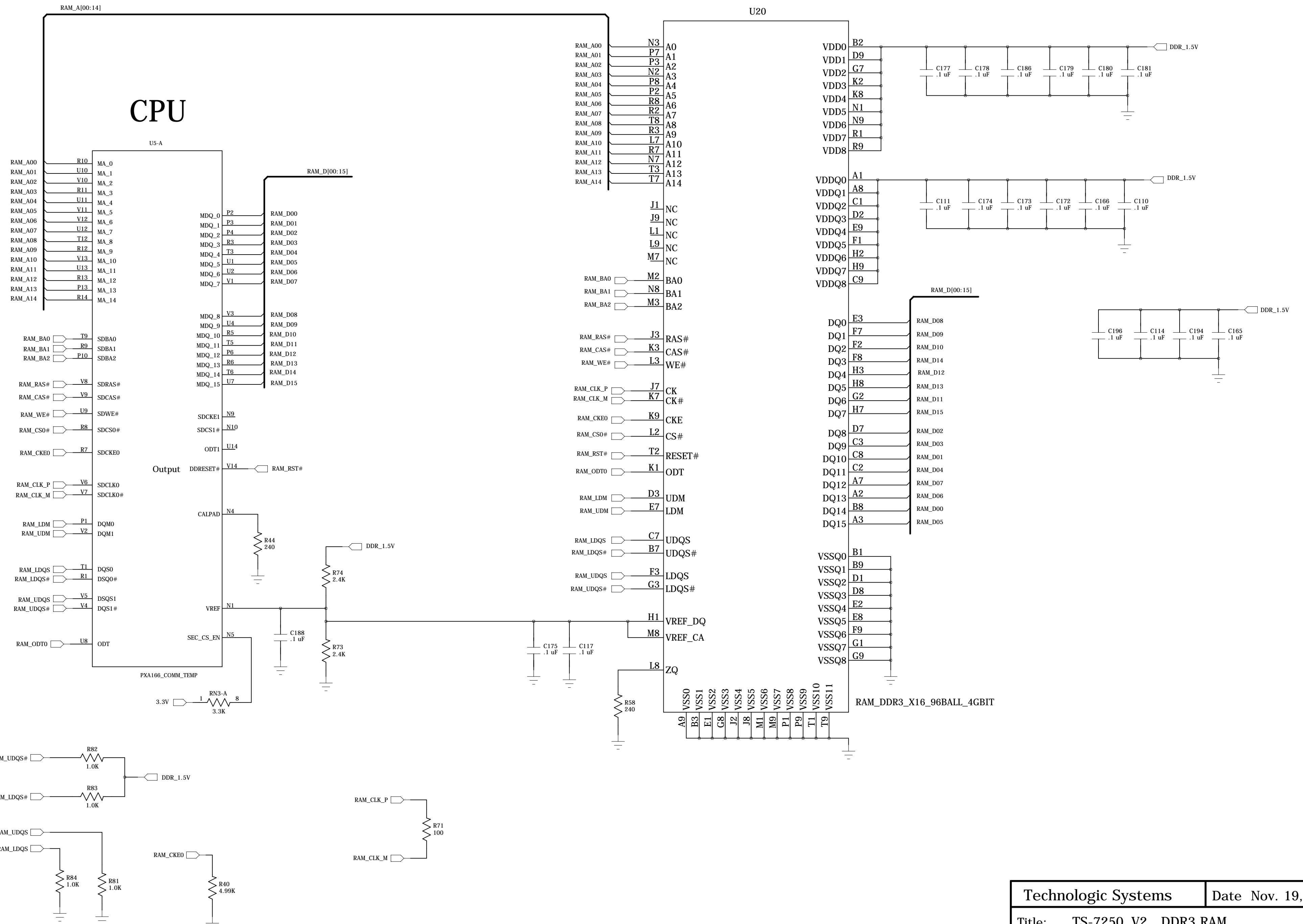
I2C

U2 = PXA166 Commercial Temp
or = PXA168 Industrial Temp

DDR3 256Mx16 RAM

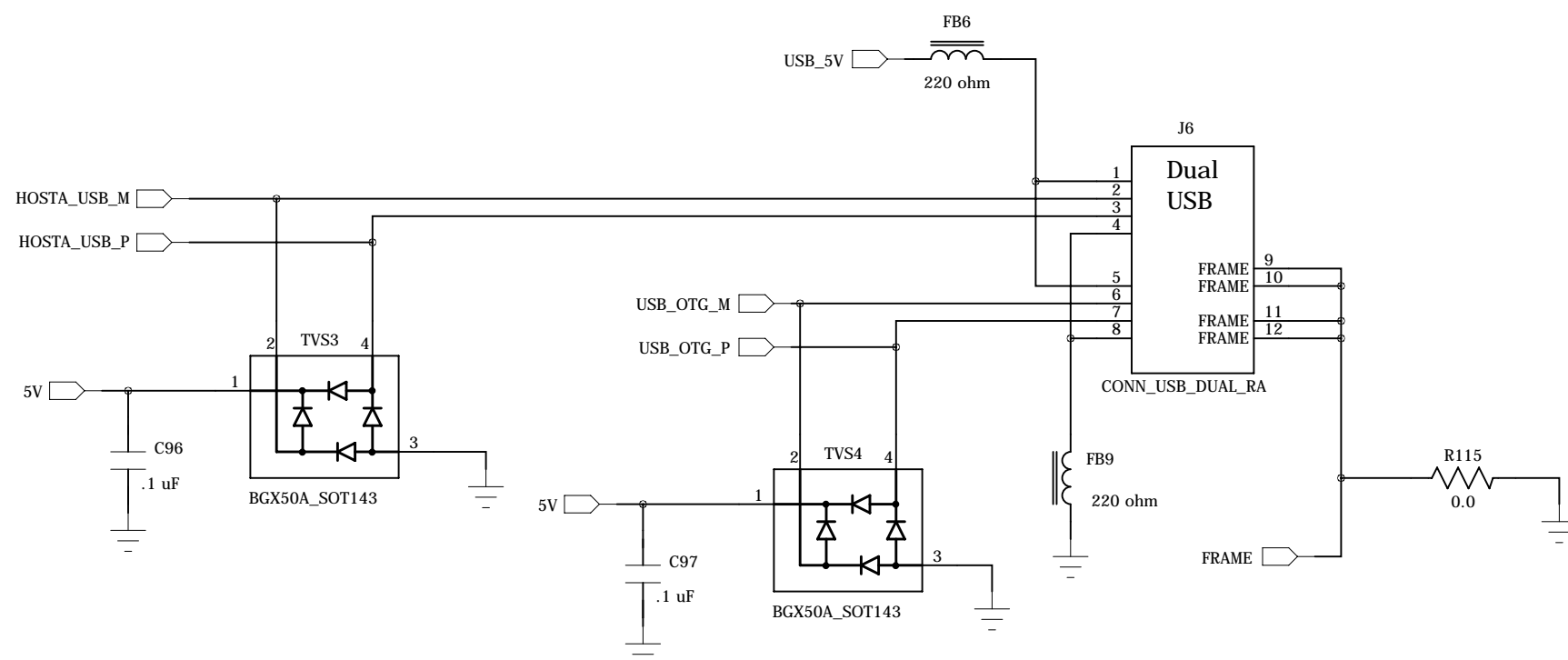
4 Gbit RAM chip

512 MB RAM

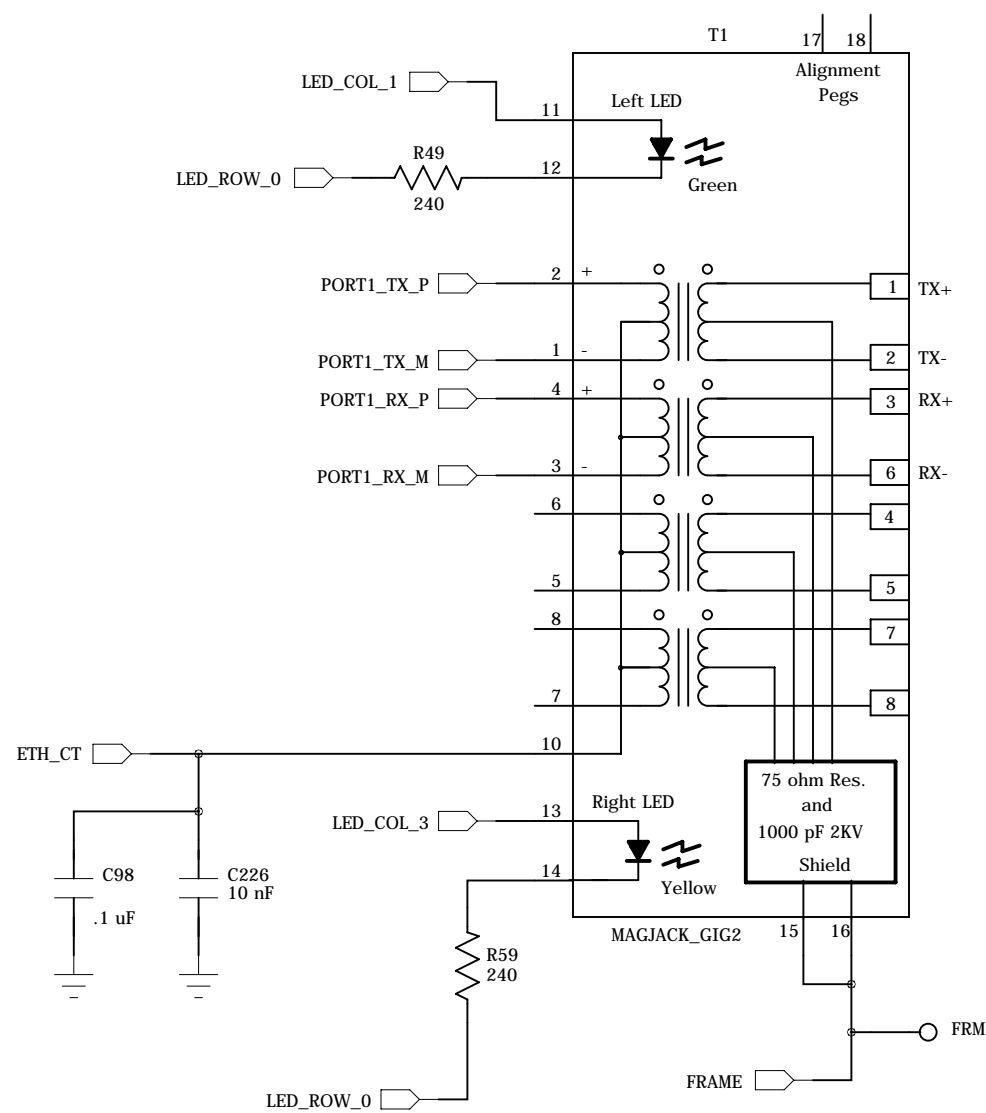


Off-Board Connectors

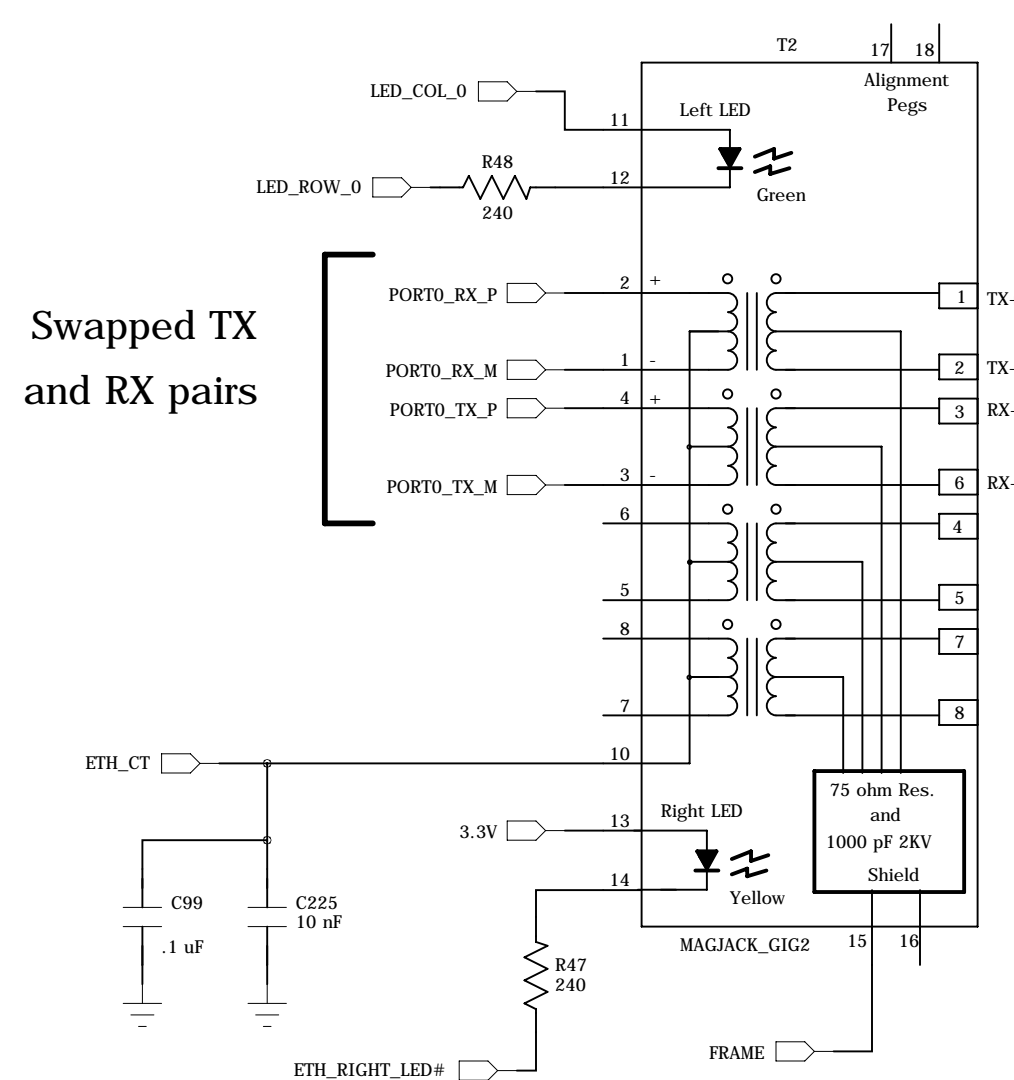
Dual Host USB Ports



Primary MagJack



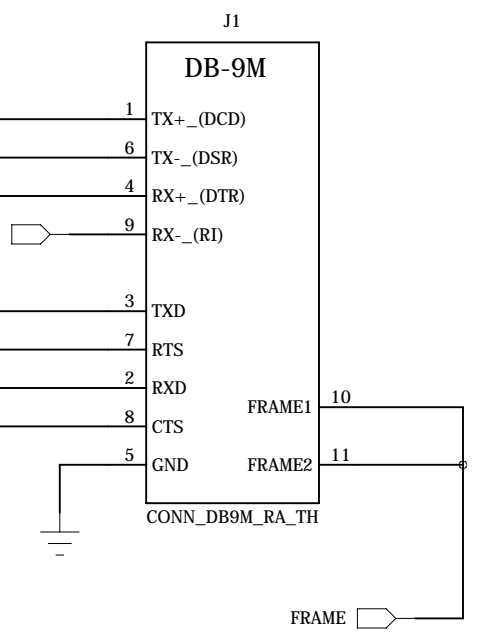
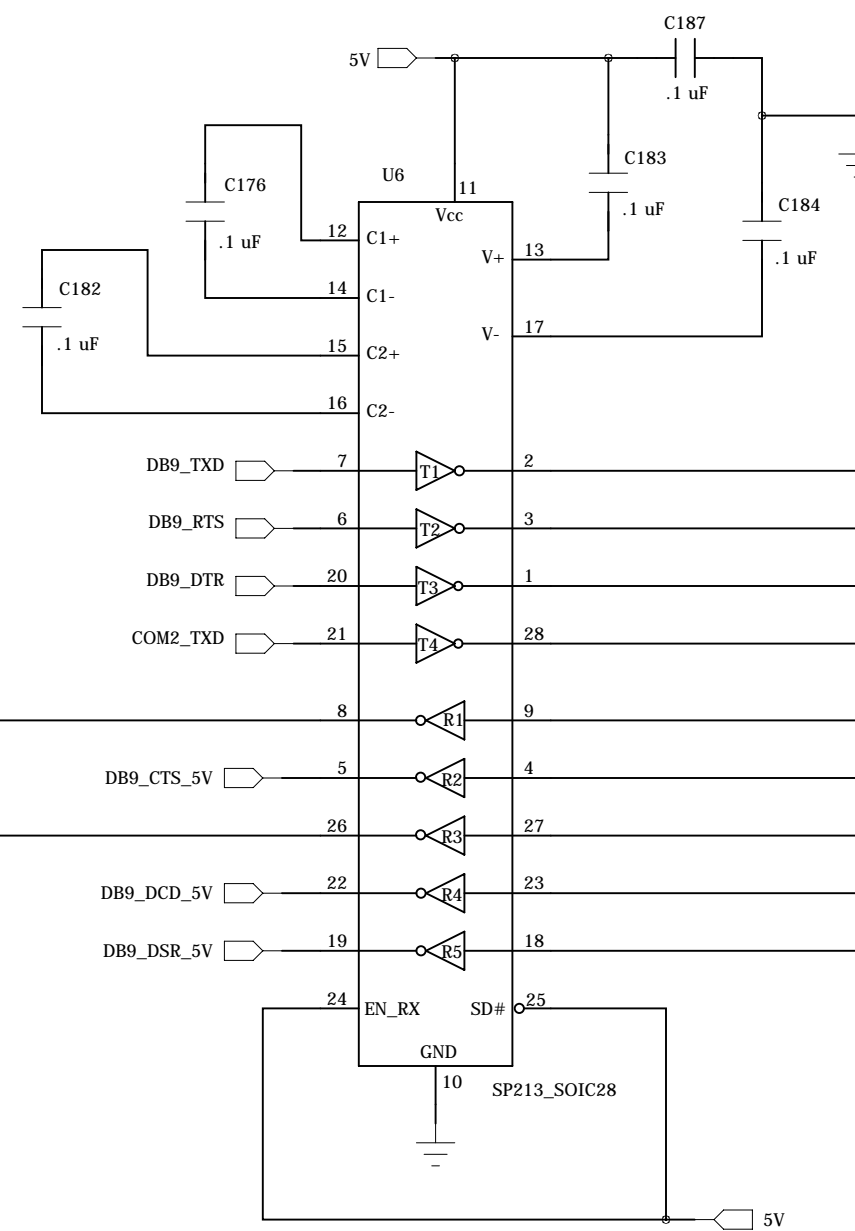
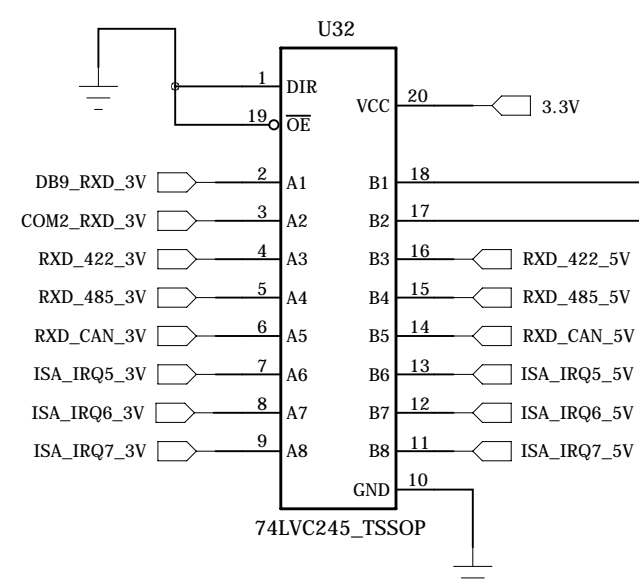
Second MagJack



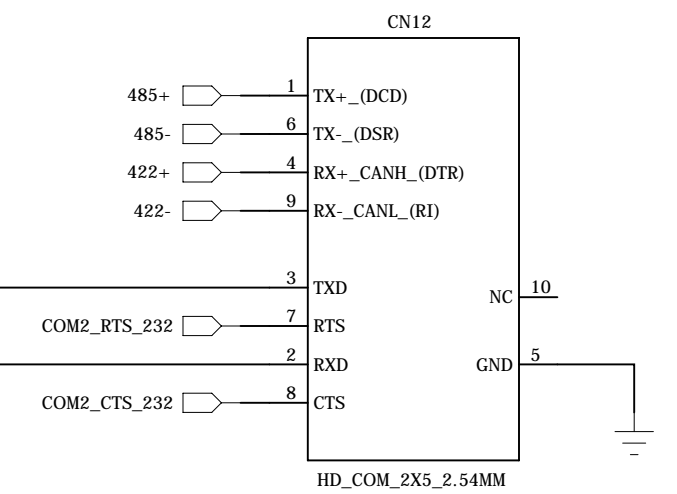
RS-232 Transceiver

DB-9M

3.3V <-- 5V
Level shifter



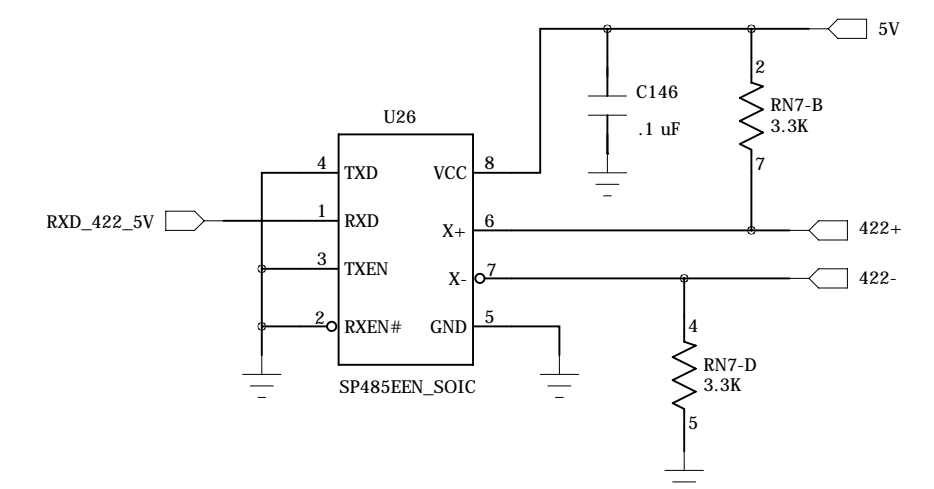
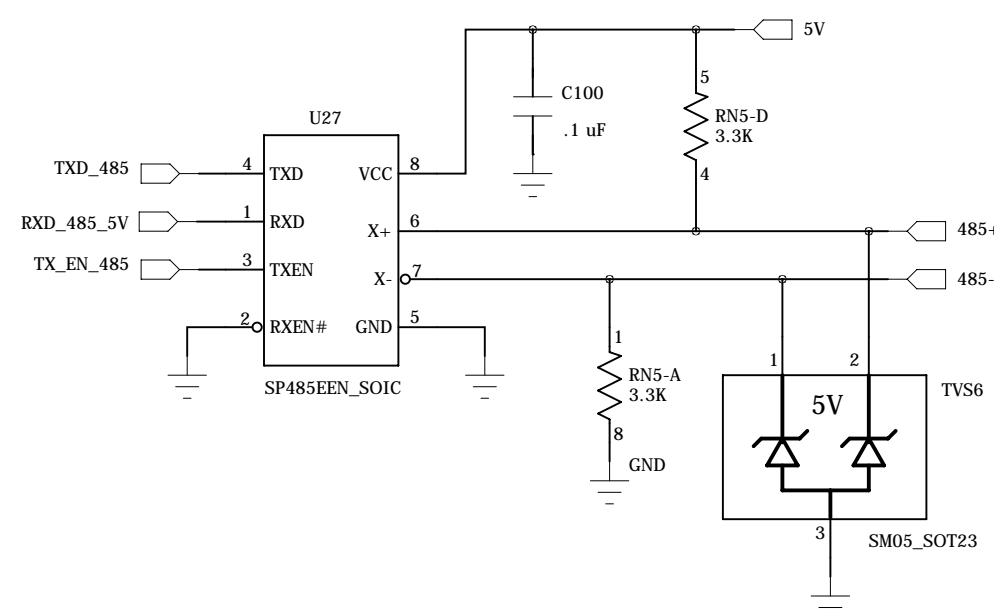
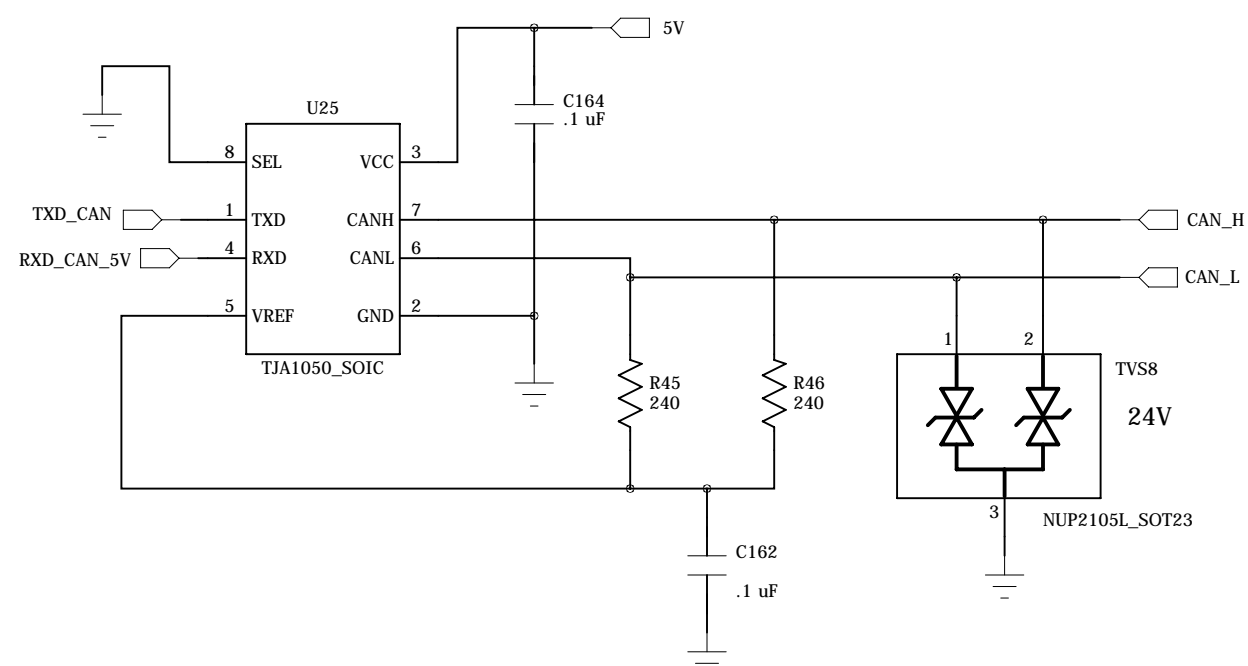
COM2 Header



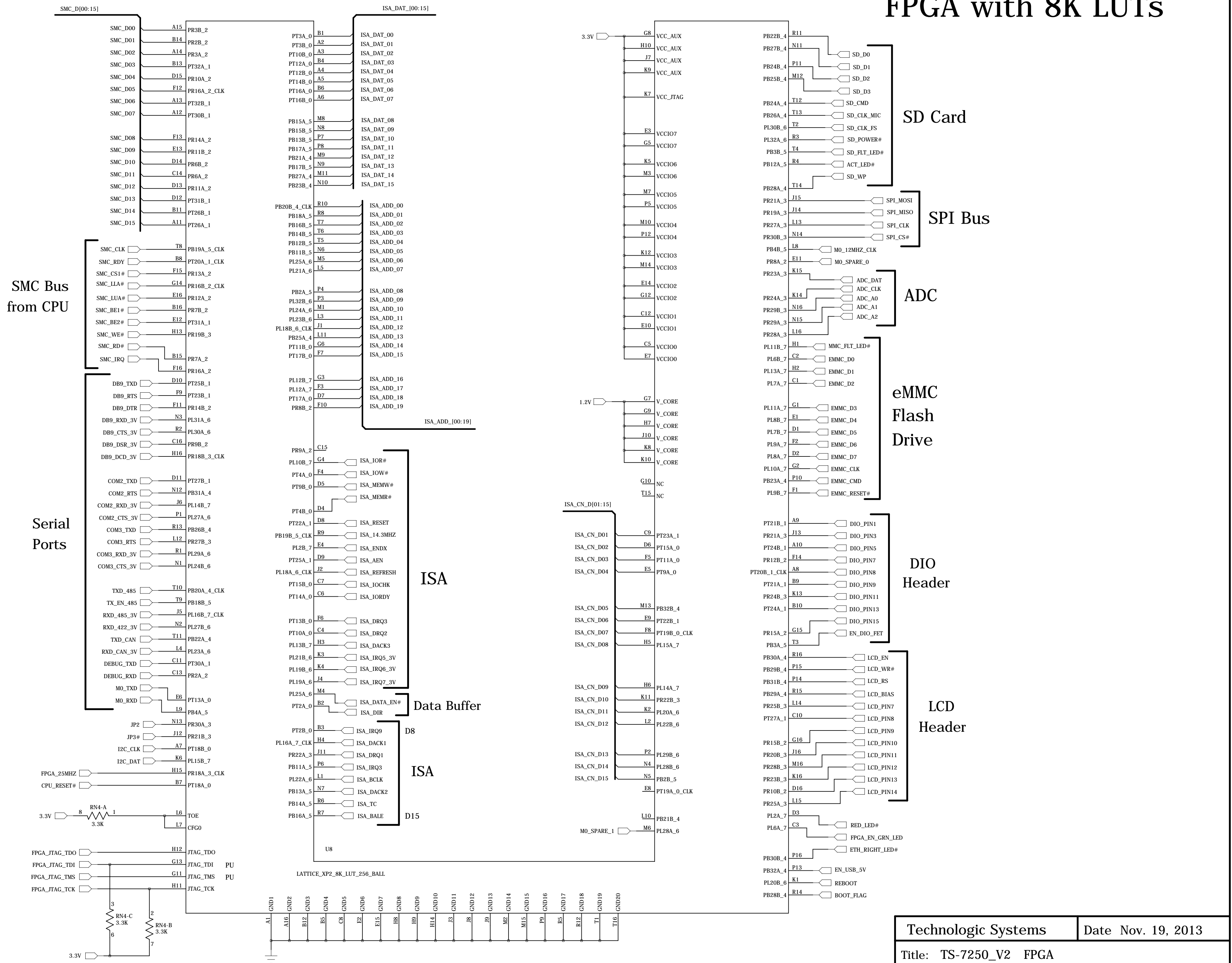
CAN Transceiver

RS-485 Transceiver

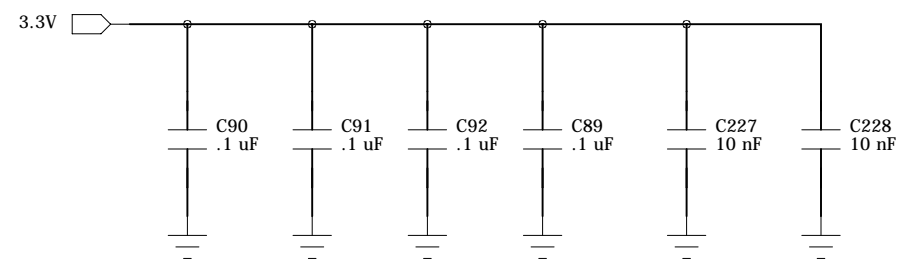
RS-422 Receiver



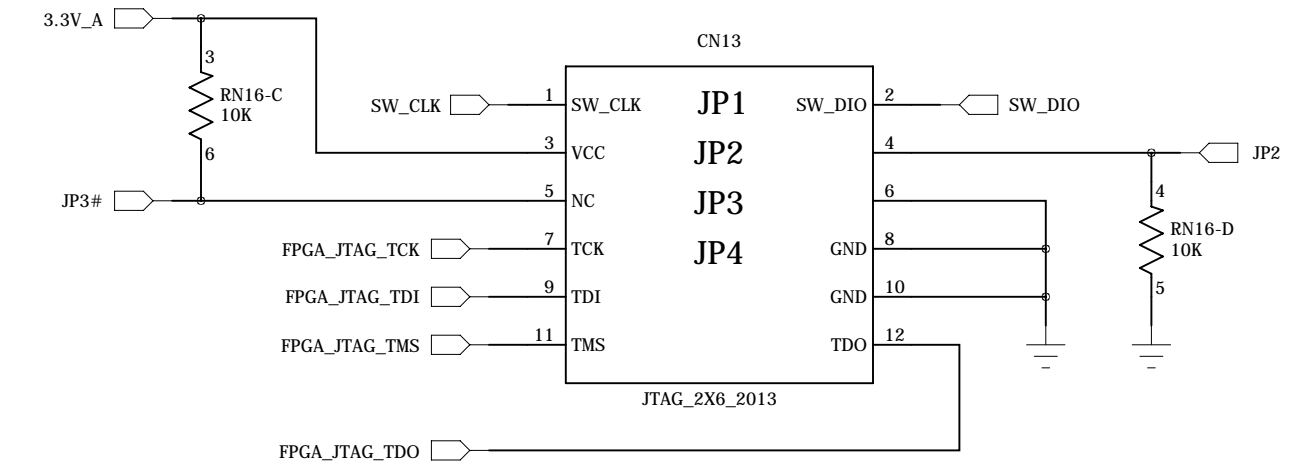
FPGA with 8K LUTs



FPGA Caps



JTAG Header

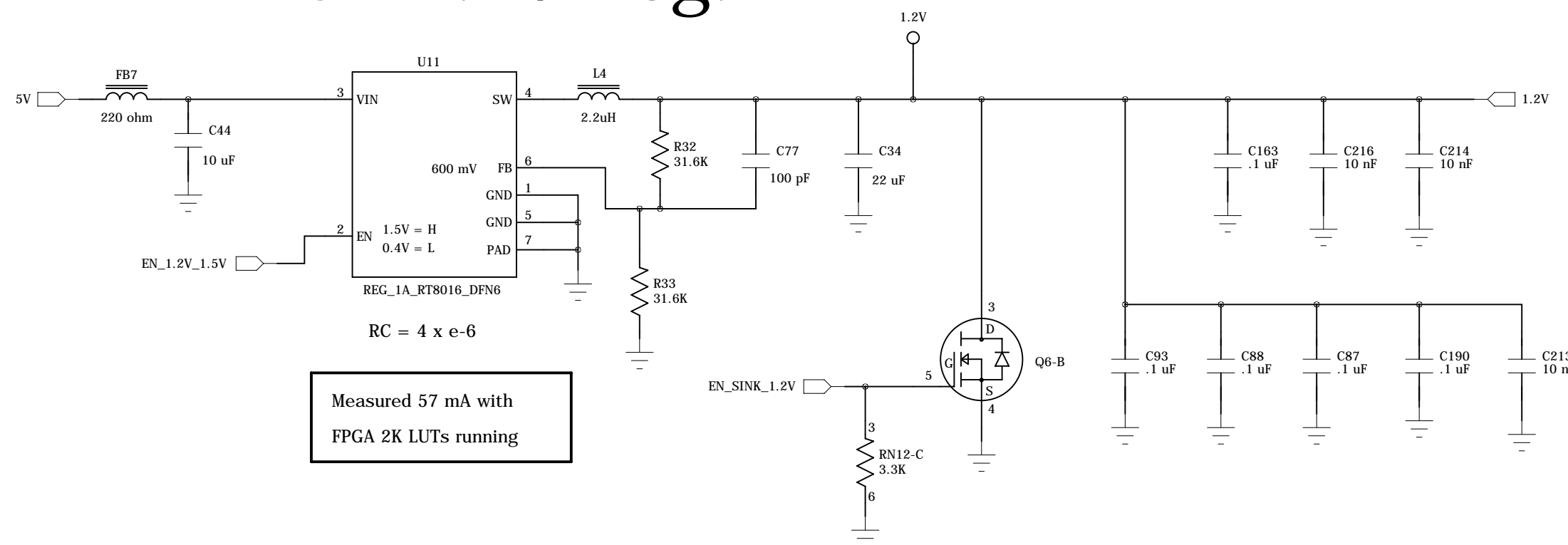


Jumpers:

- JP1 = ??
- JP2 = SD Boot
- JP3 = Console --> DB9
- JP4 = User

If JP4 installed
CPU can not reload FPGA

#4 FPGA 1.2V Reg.



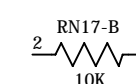
Measured 57 mA with
FPGA 2K LUTs running

Page 37 of Data Sheet (Hot Socketing)
FPGA Power Supplies can be sequenced in any order but must be monotonic
All I/O lines are tri-stated during power cycling

TS-7250

Jumpers:

- JP1 = Boot Serial
- JP2 = Console Enable
- JP3 = Write Enable Flash
- JP4 = Stop @ Redboot
- JP5 = TS_Test
- JP6 = Reserved

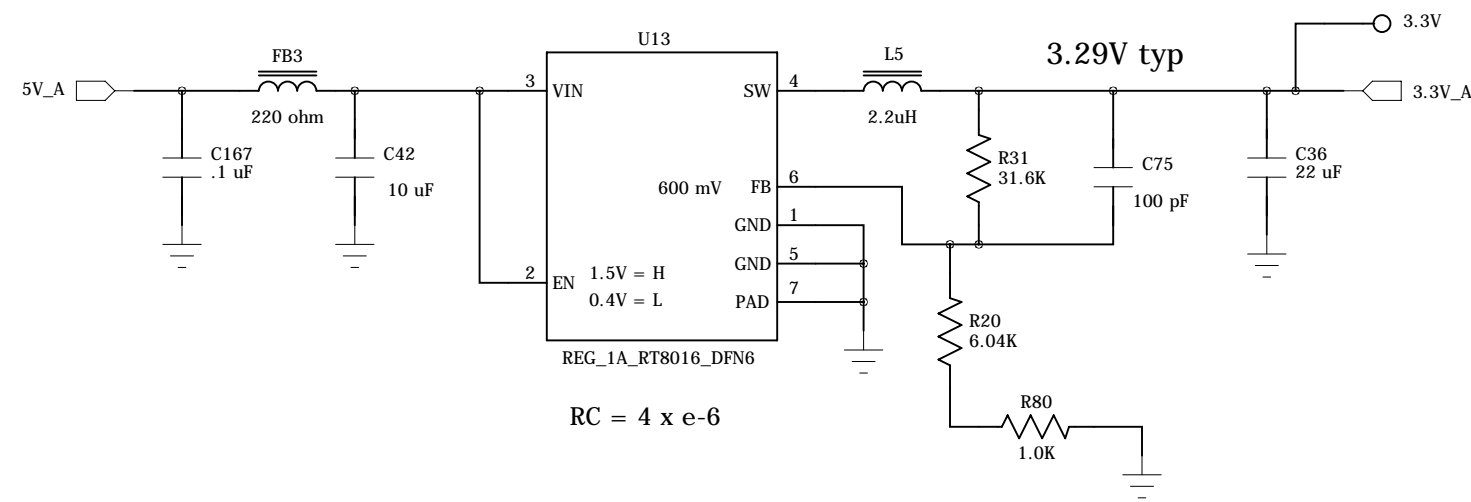


Technologic Systems	Date Nov. 19, 2013
Title: TS-7250_V2 FPGA PS, JTAG	
Rev: A	Designer
Sheet 7 of 16	

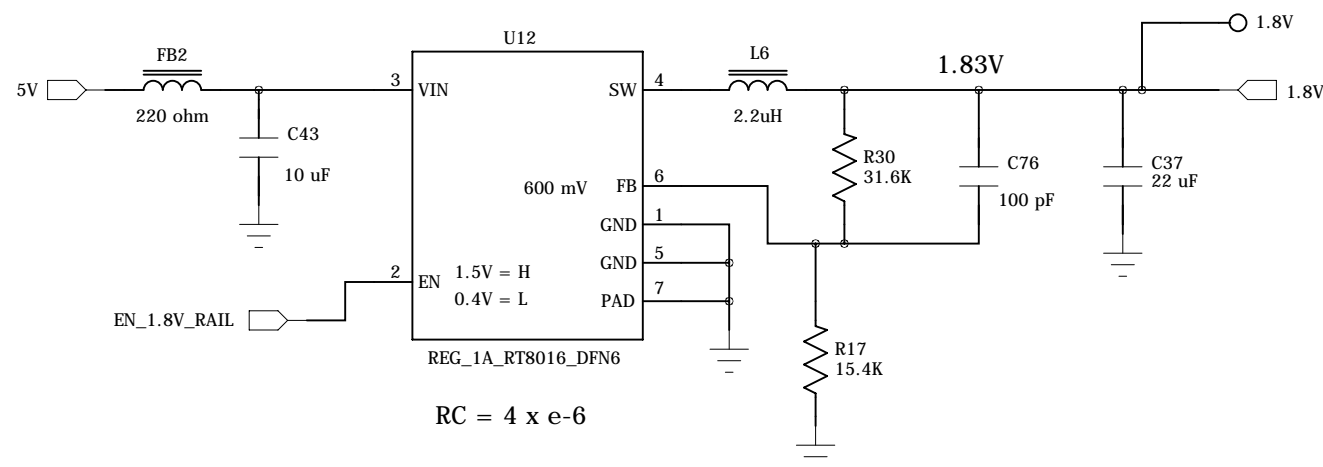
Power Supplies

#1 3.3V Power Supply

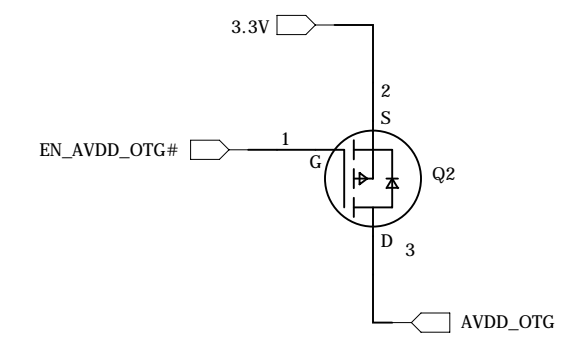
up to 1000 mA



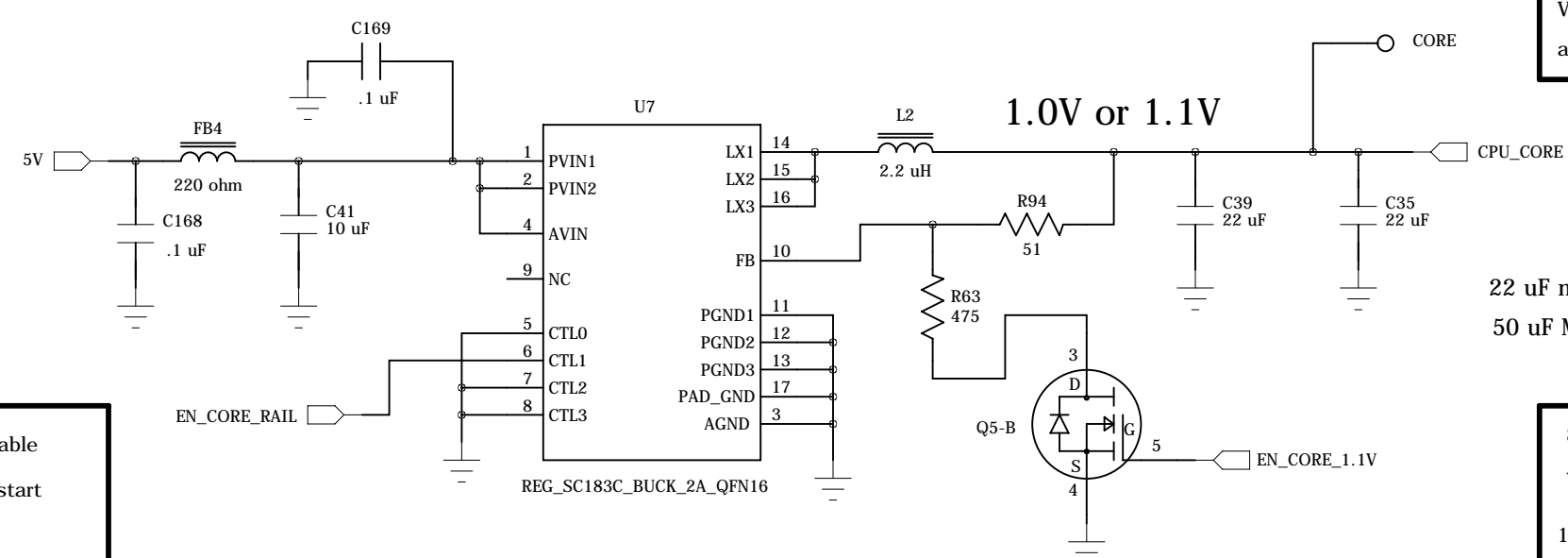
#2 1.8V Regulator



#5 CPU USB Power



#3 CPU Core Supply



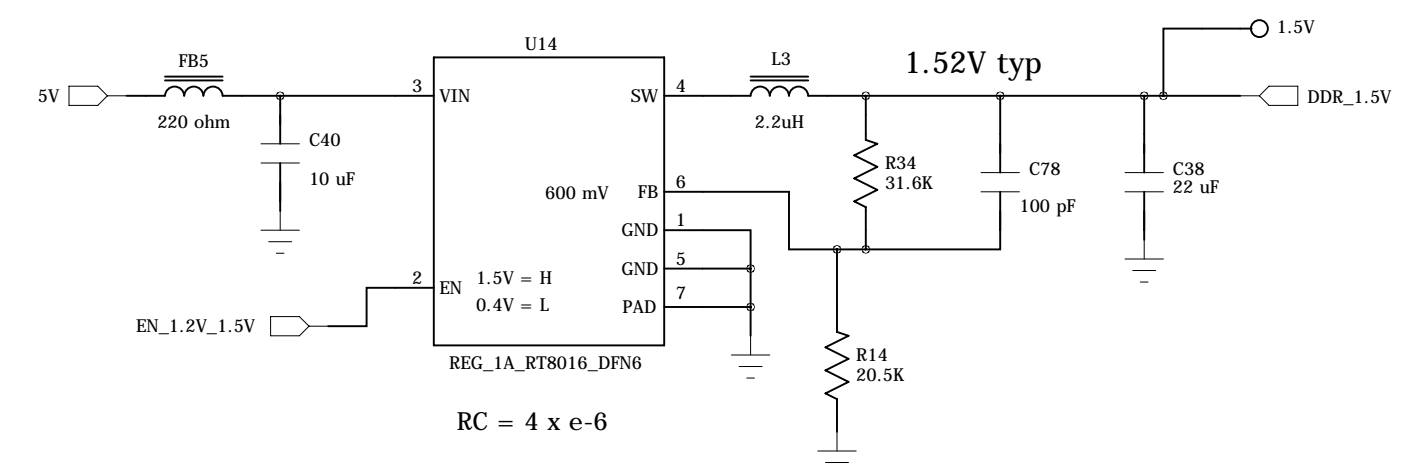
Vout rise time
about 130 us

22 uF minimum
50 uF Max.

800 MHz CPU needs
Vcore = 1.00V
1000 MHz needs 1.10V

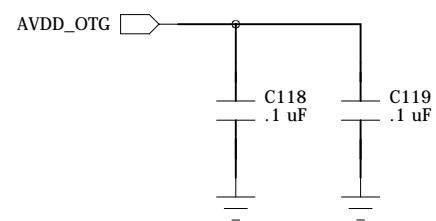
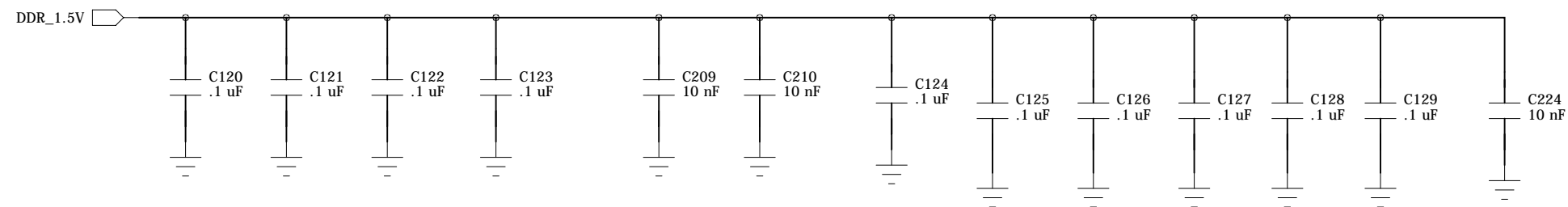
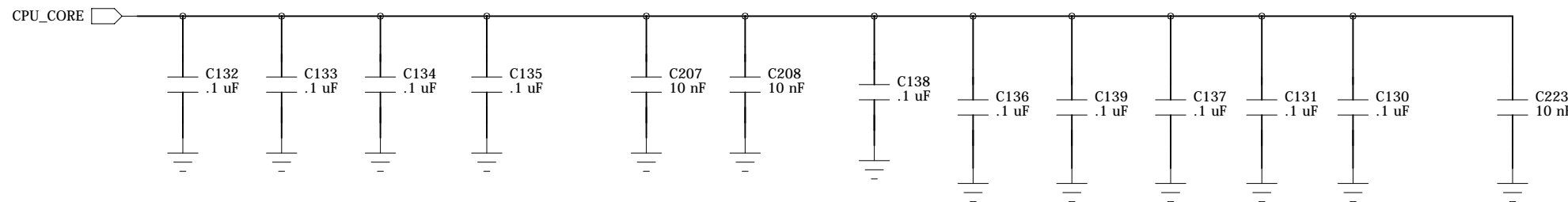
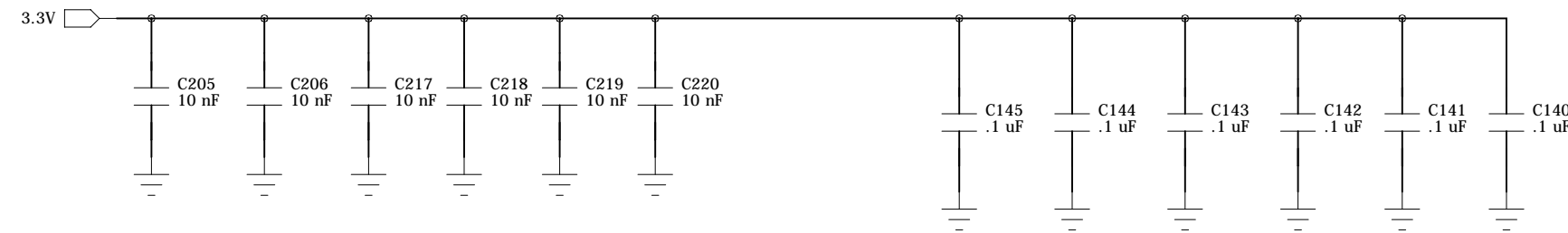
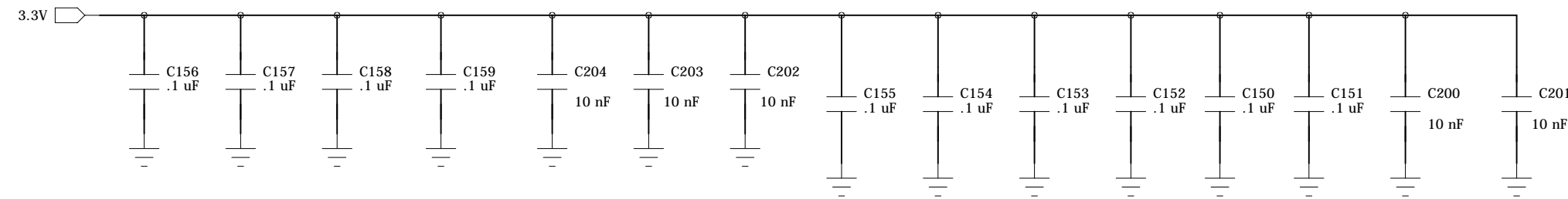
Delay from Enable
to Vout ramp start
is typ. 50 us

#4 DDR3 1.5V Reg.

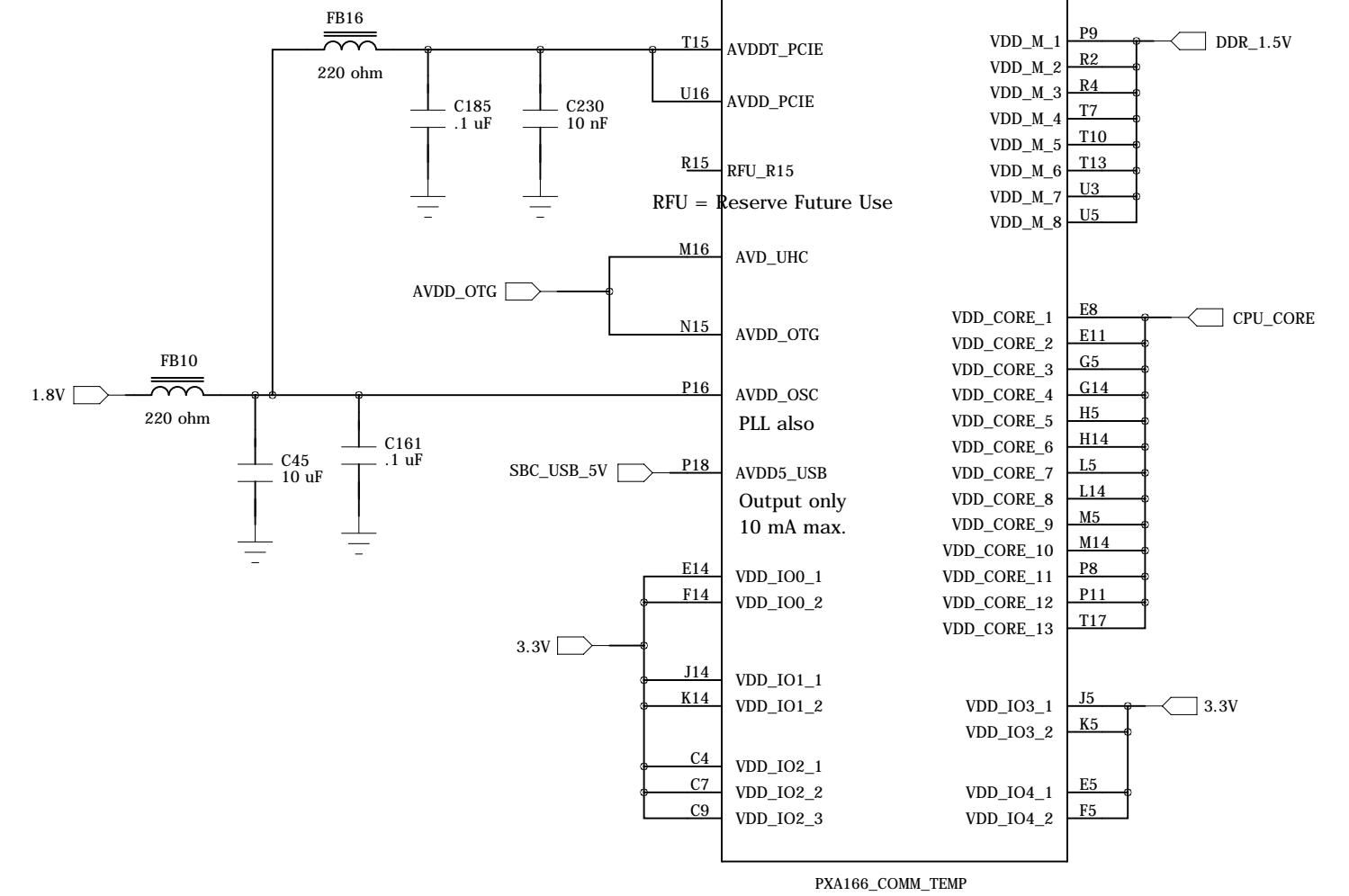


Technologic Systems	Date Nov. 19, 2013
Title: TS-7250_V2 Power Supplies	
Rev: A	Designer
Sheet 8 of 16	

CPU Power



PXA168 PCIe rails must be connected to AN_1.8V



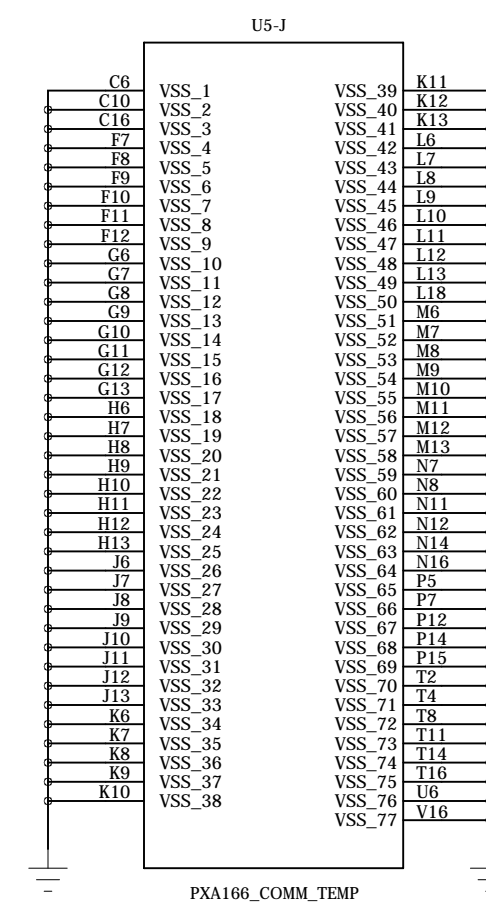
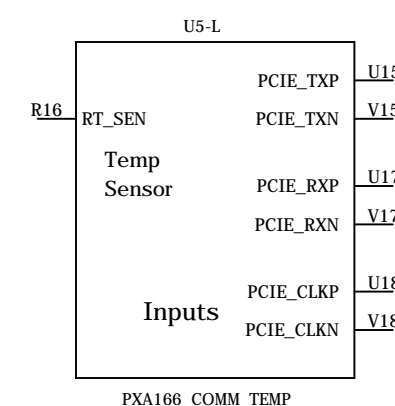
CPU

CPU

CPU PCIe

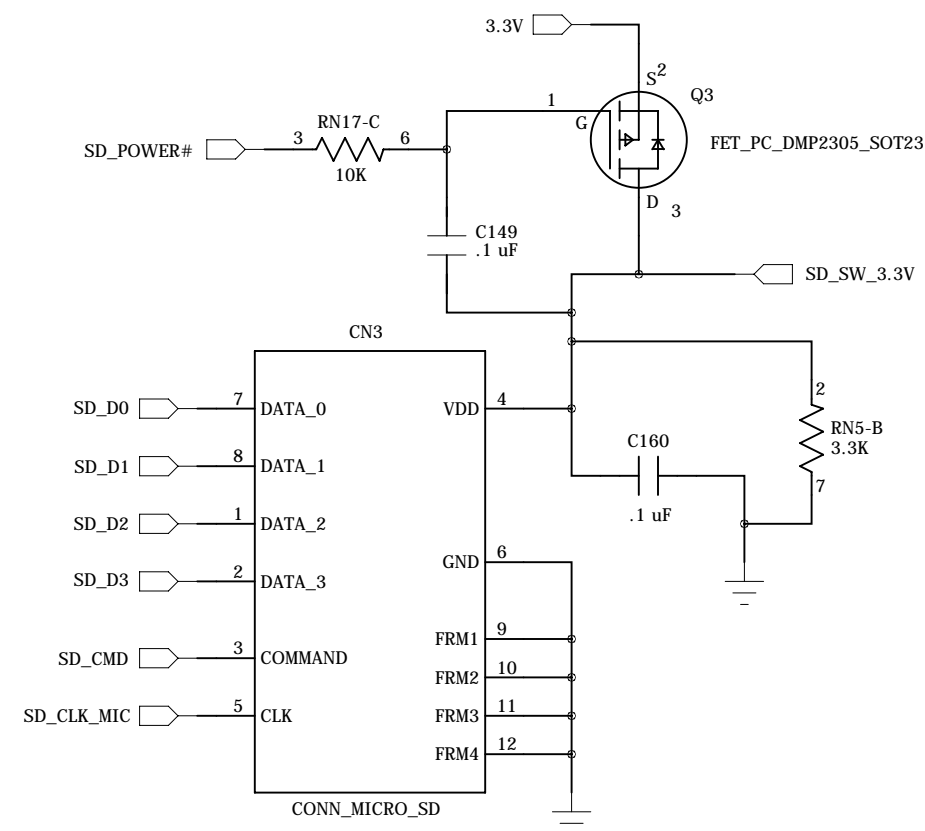
Not used

PCIe not supported on PXA166

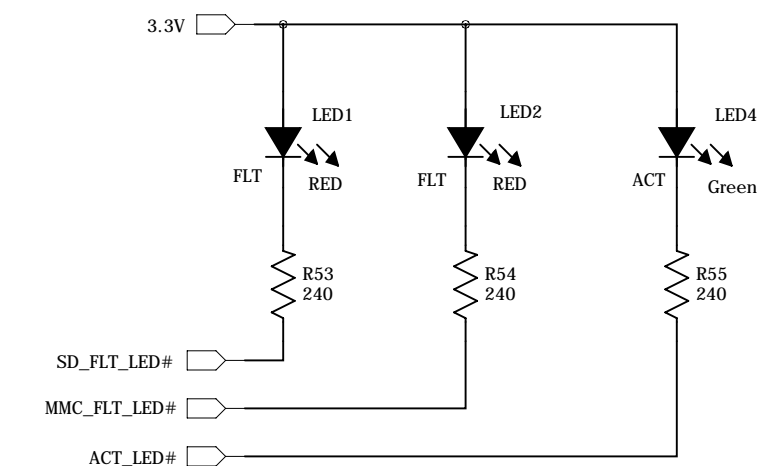


Flash Storage

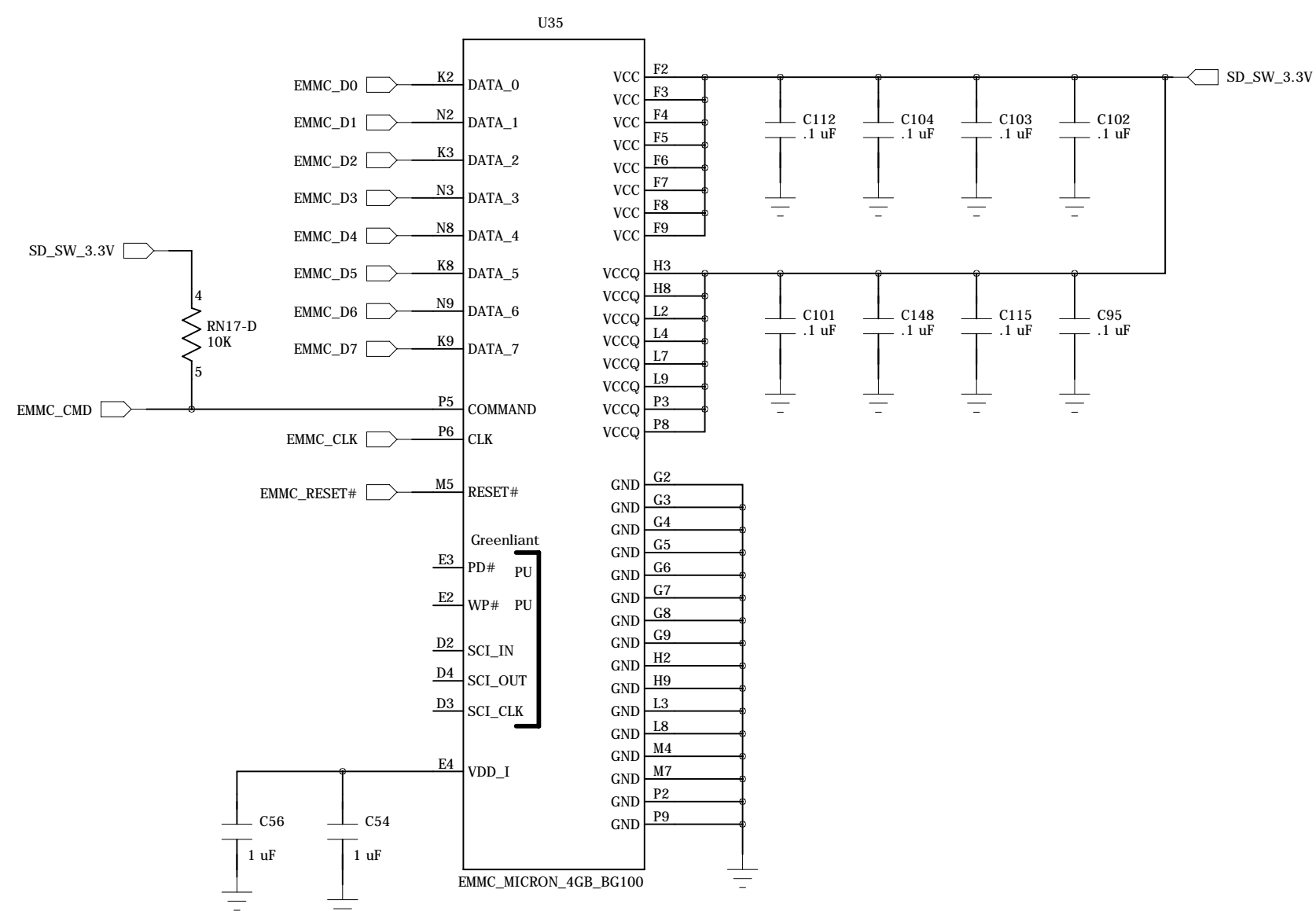
Micro SD Card Socket



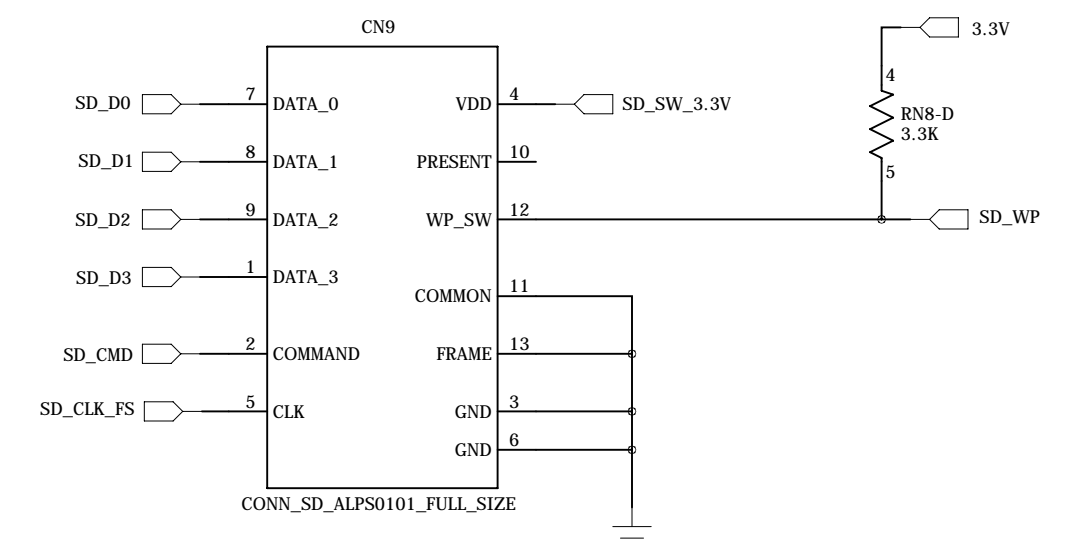
SD Card LEDs



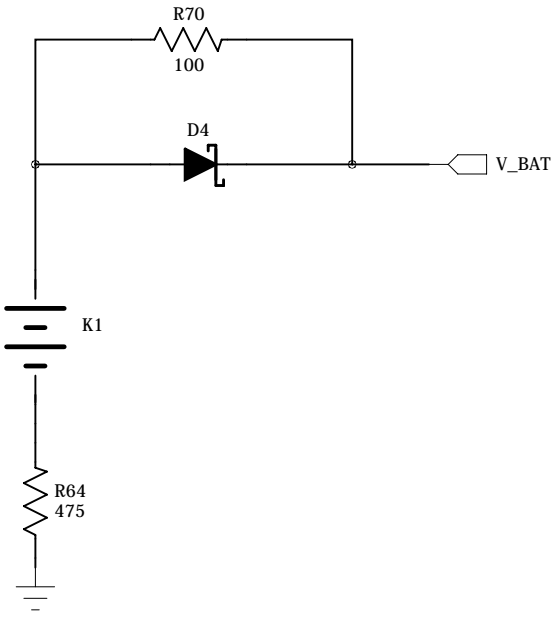
eMMC 4GB



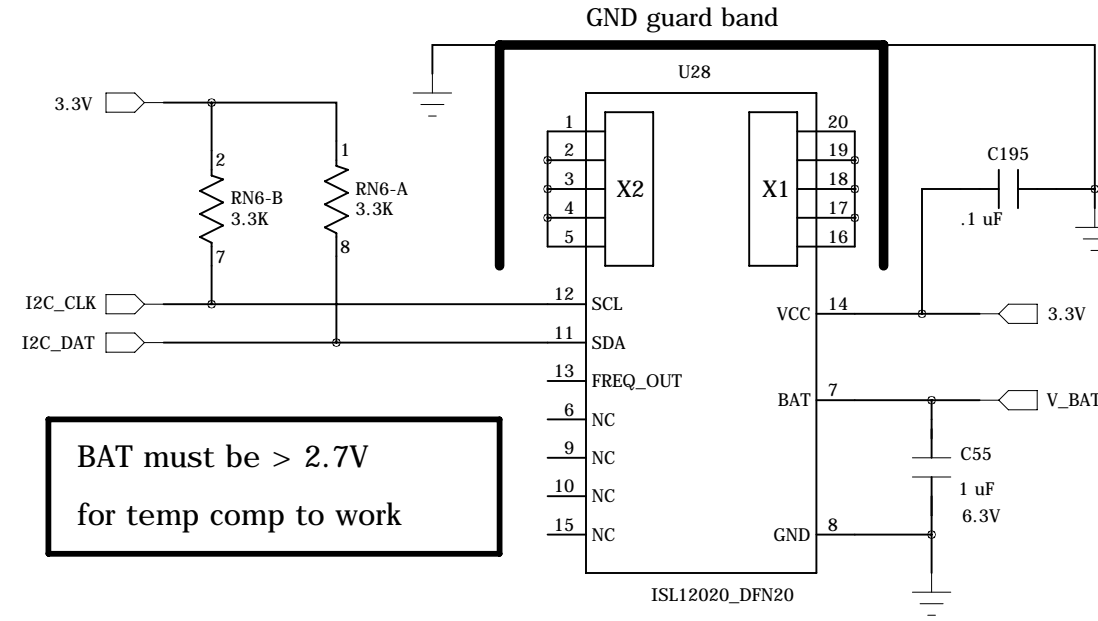
Full Size SD Socket



RTC Battery



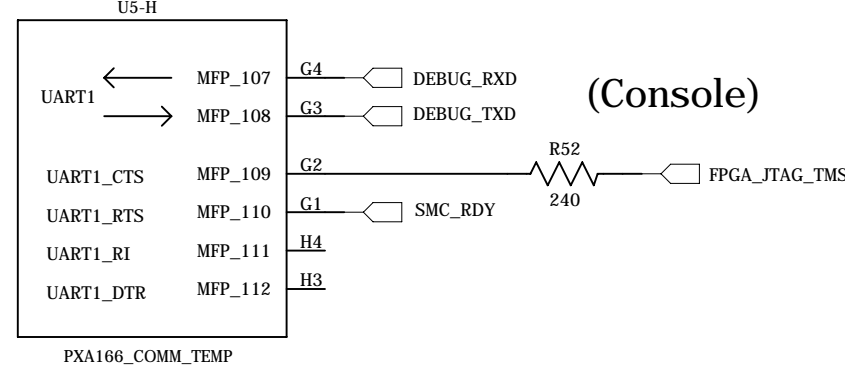
RTC and Temp. Sensor



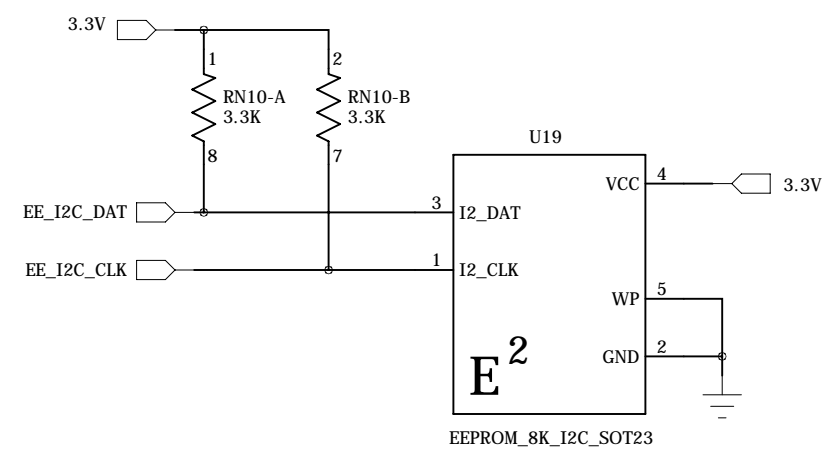
BAT must be > 2.7V
for temp comp to work

Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

CPU Debug UART

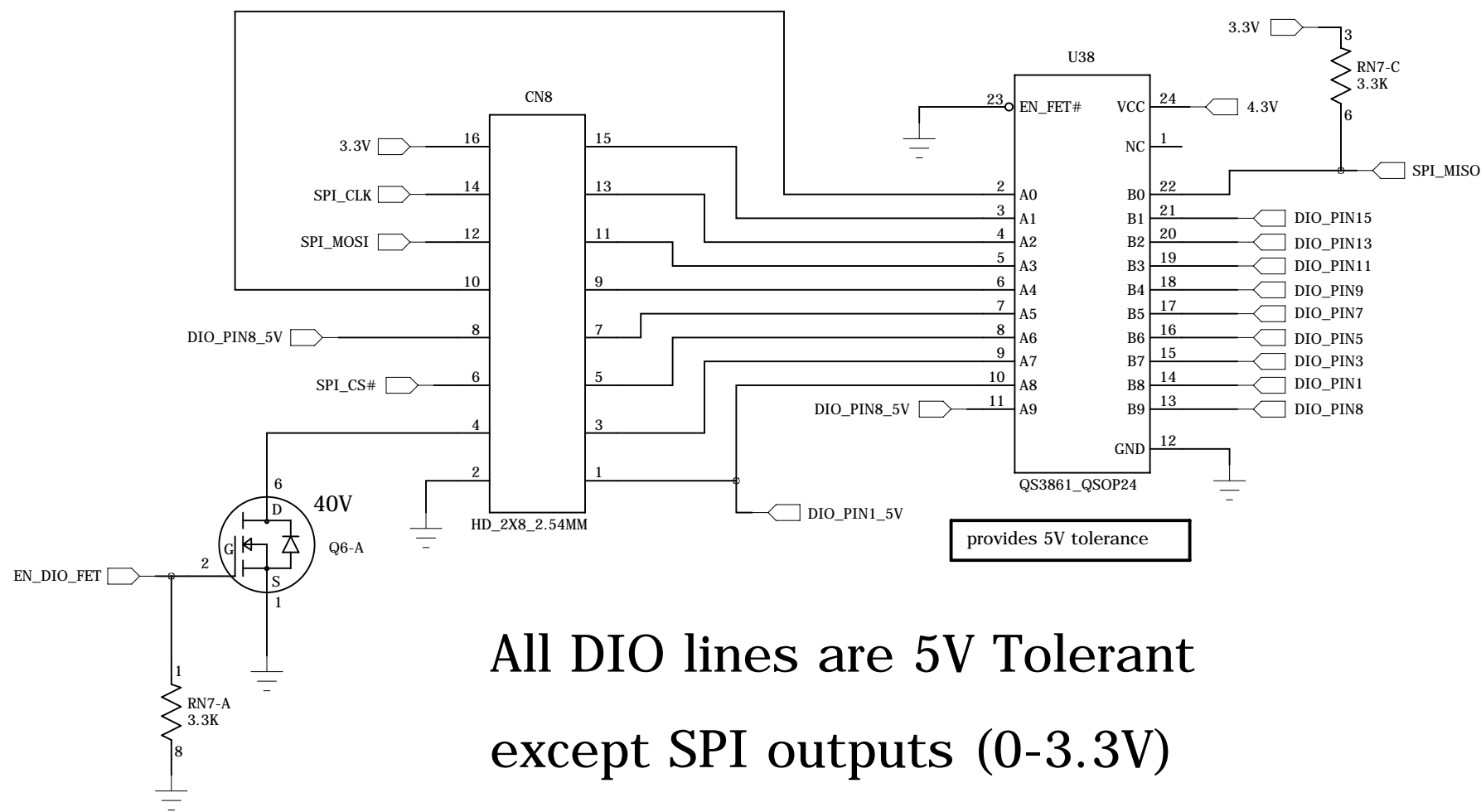


EEPROM 1 Kbyte



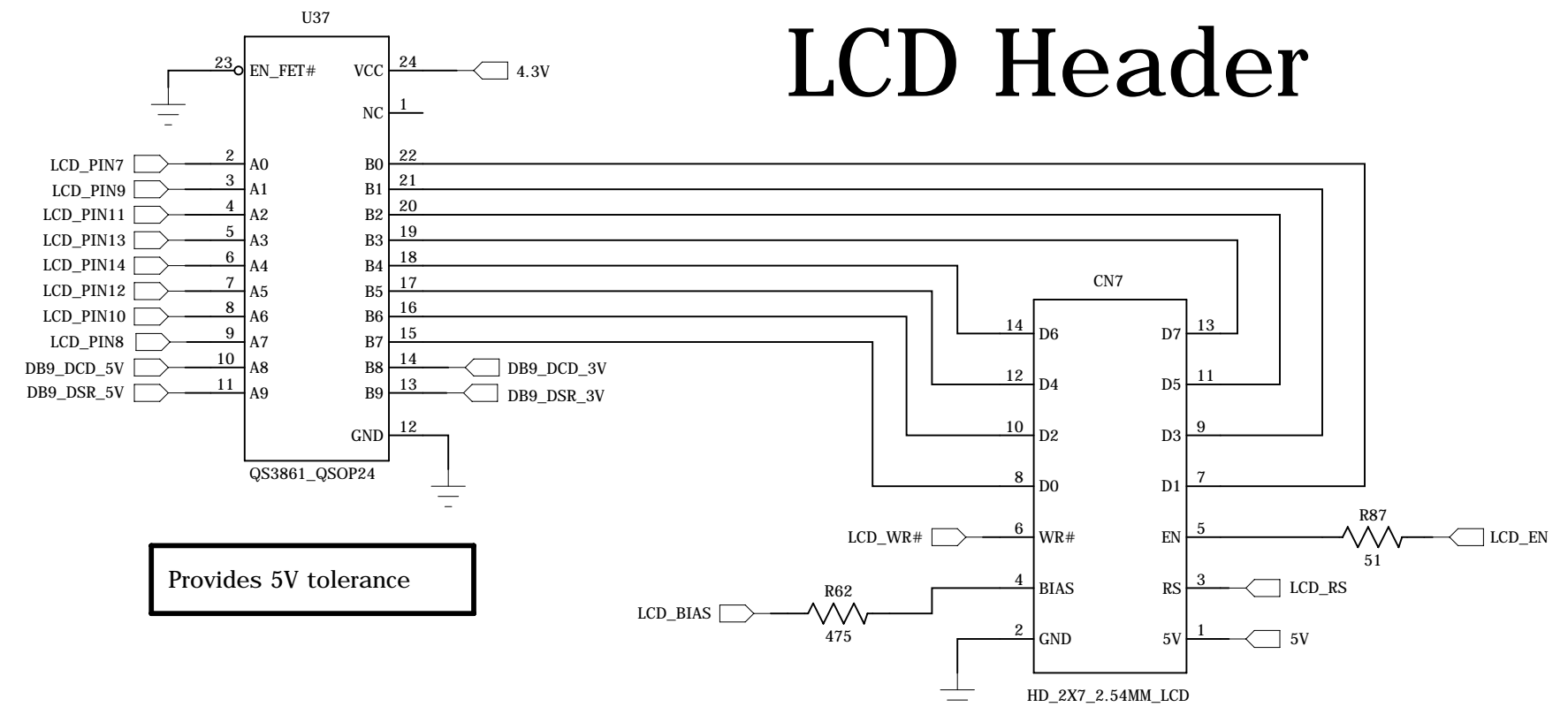
DIO and LCD Headers

DIO Header



All DIO lines are 5V Tolerant
except SPI outputs (0-3.3V)

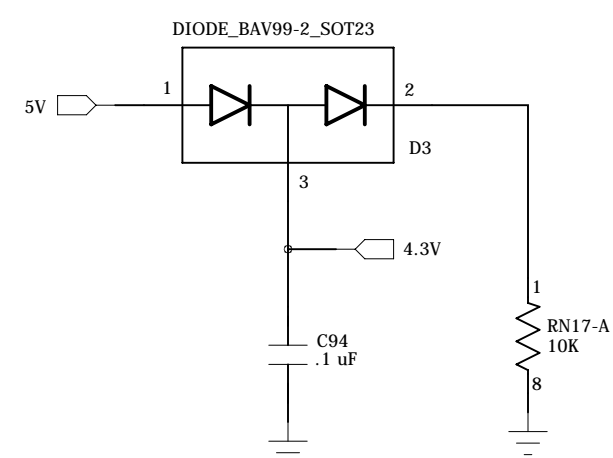
LCD Header



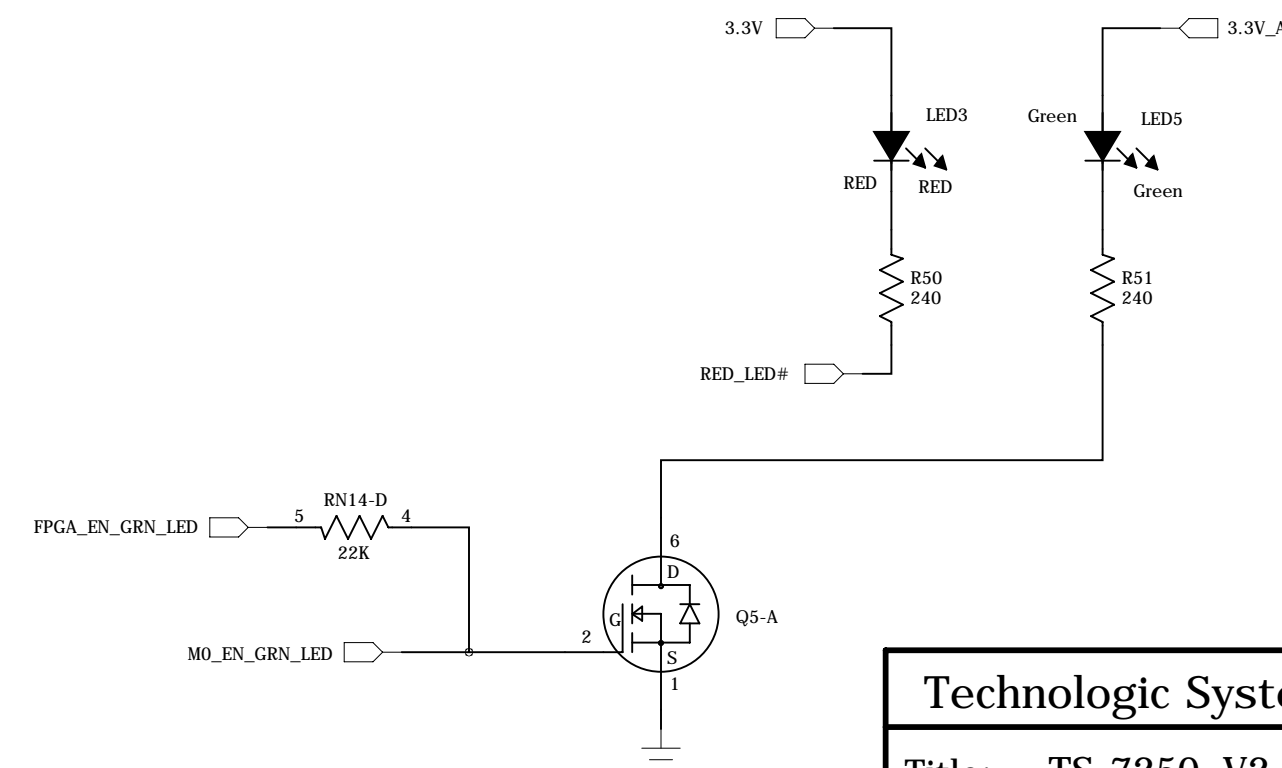
LCD Data lines are 5V tolerant

All LCD pins are
bi-directional DIO

4.3V Supply

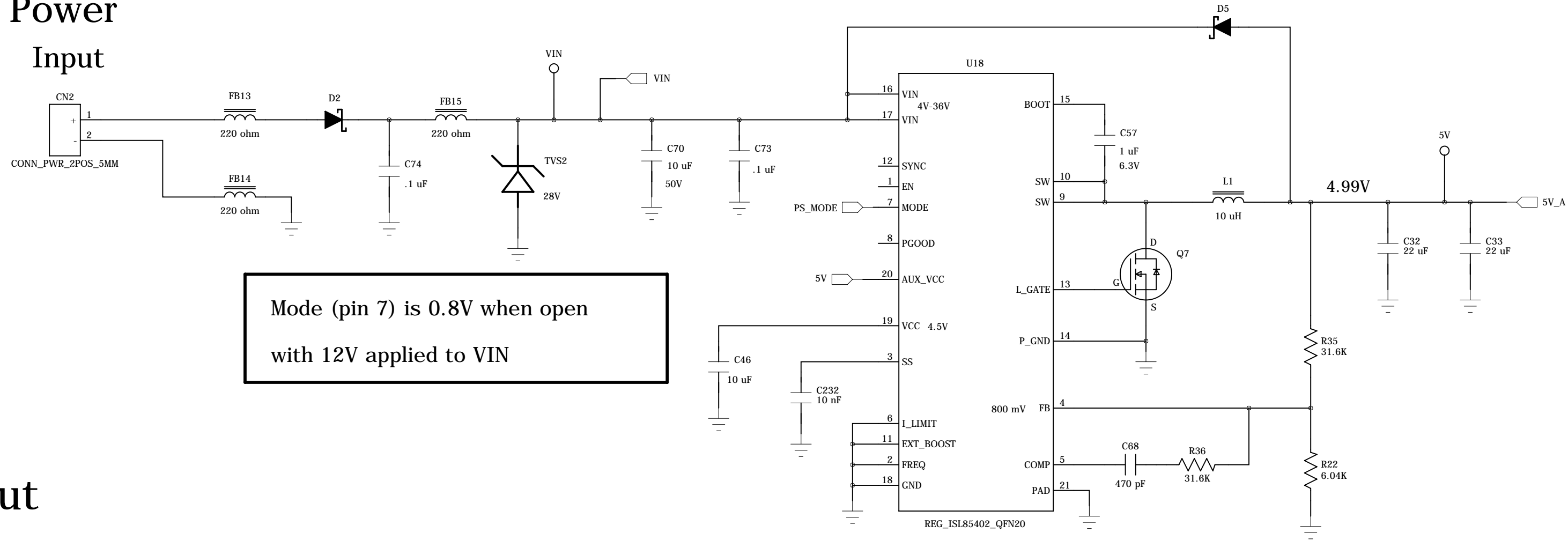


Red and Green LEDs



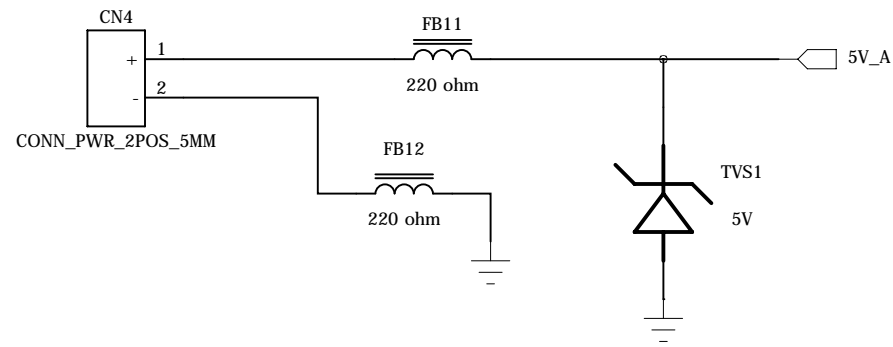
5V Power Supply (2000 mA)

8V-28V
Power
Input

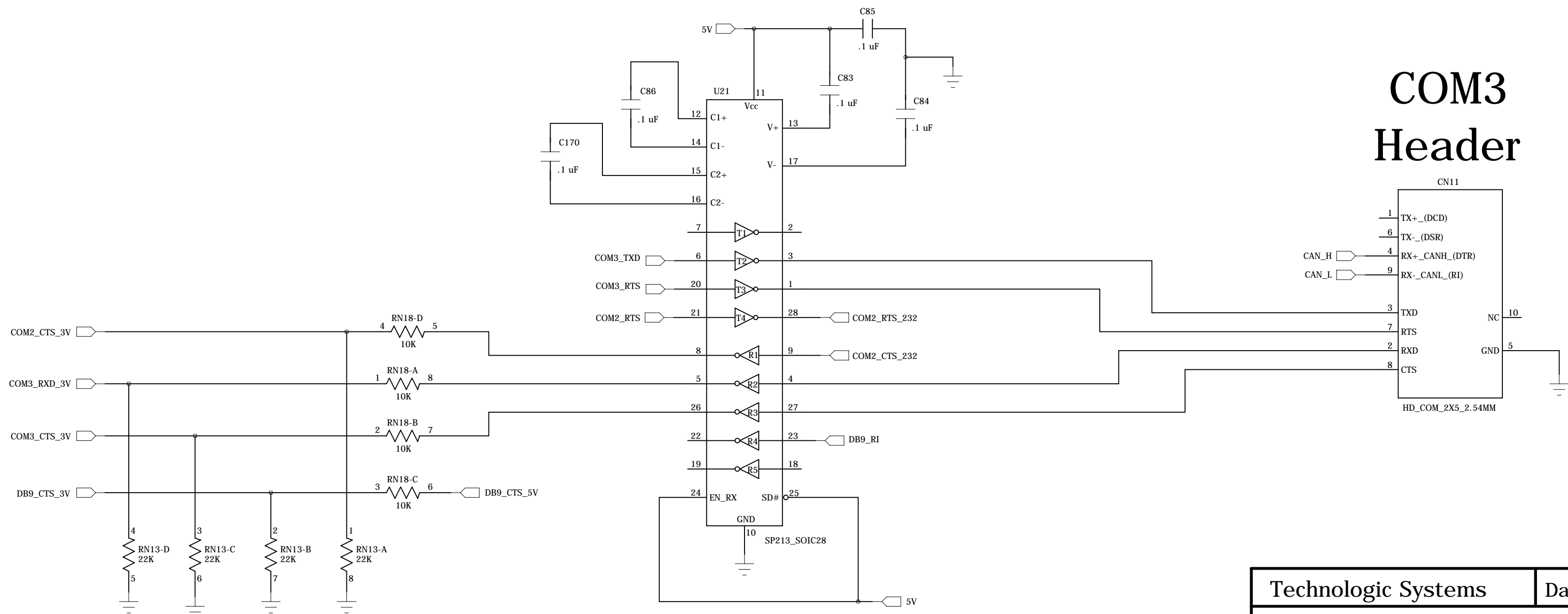


Mode (pin 7) is 0.8V when open
with 12V applied to VIN

5V Input



RS-232 Transceiver

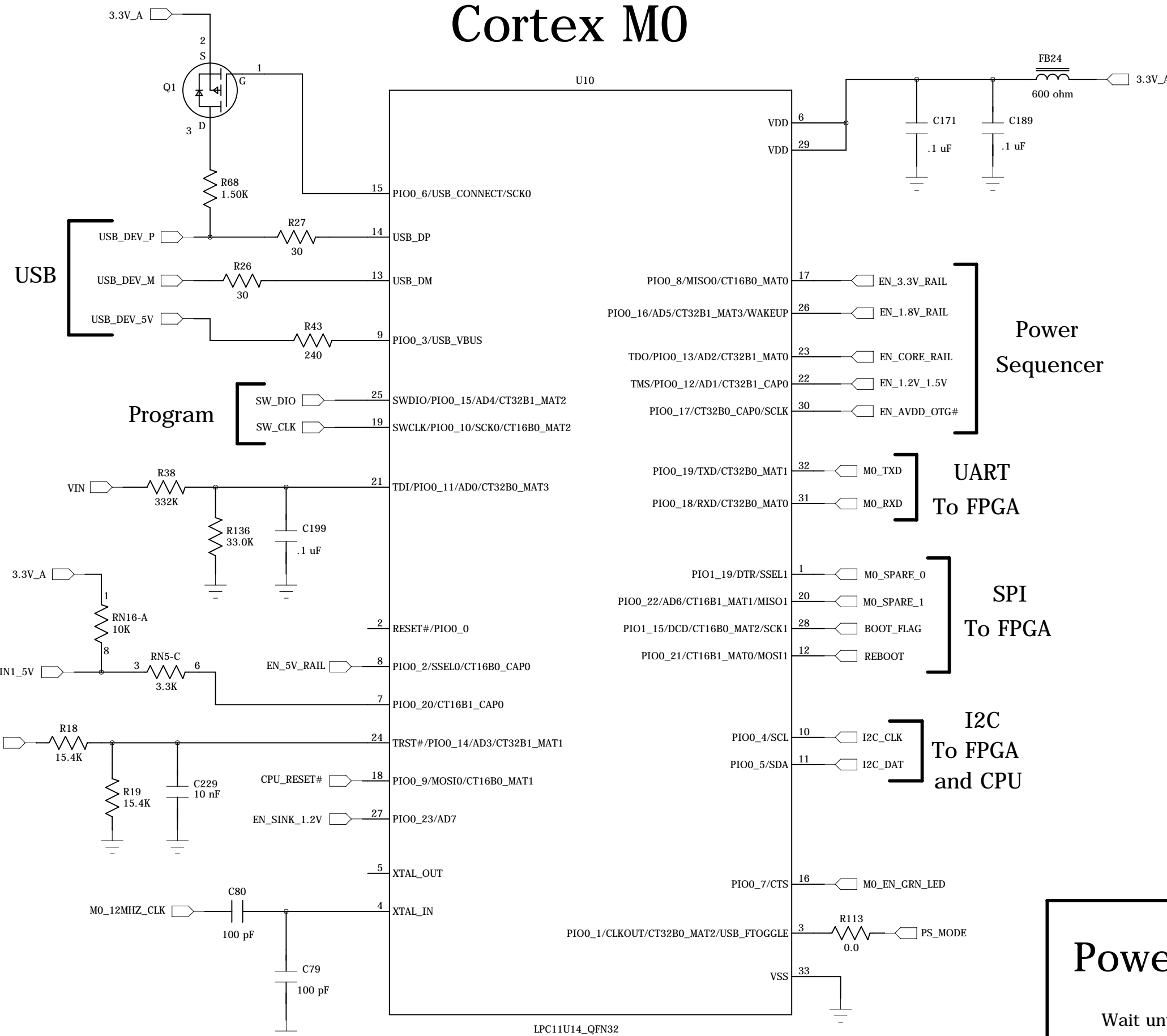


COM3
Header

Technologic Systems	Date Nov. 19, 2013
Title: TS-7250_V2 5V Regulator	
Rev: A	Designer
Sheet 13 of 16	

USB Device Port and Cortex M0

Cortex M0



Pins 2 and 3 must be high at Pwr up

DIO pin 1, SW_CLK, or SW_DIO can be used for M0 "Wake up"

To test JP1, set SW_DIO low for 2 us read SW_CLK, then tri-state SW_DIO

Power Sequencer

Wait until 5V_A rail > 4.2V for 80 ms, then start sequencing

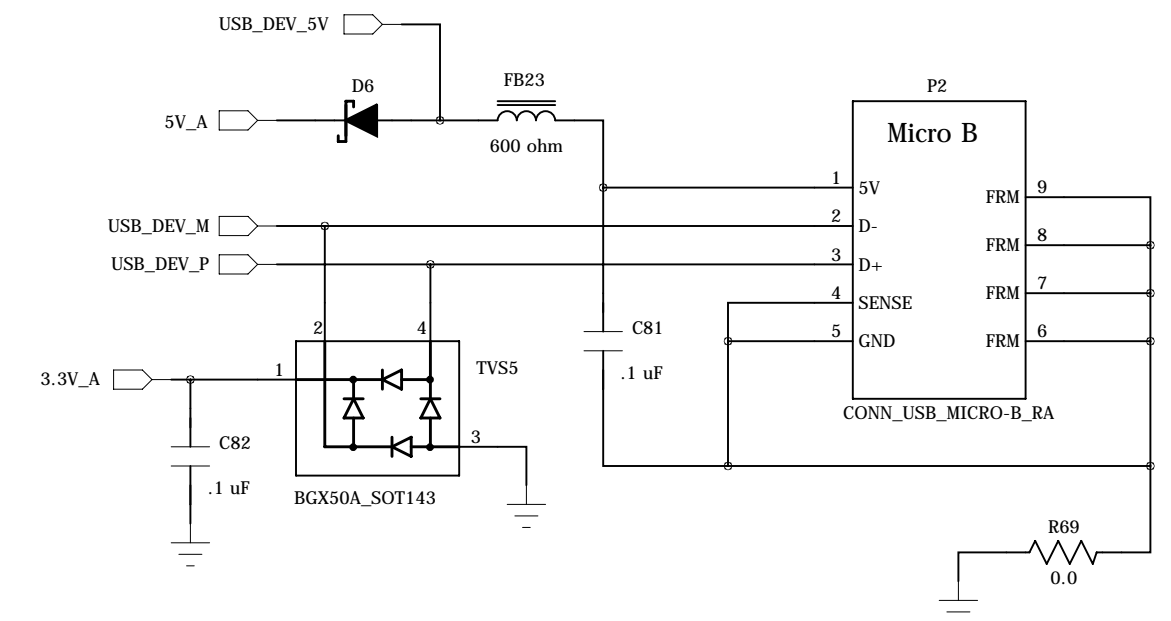
Delay:

- 5 ms 1 - Enable 5V Rail
- 5 ms 2 - Enable 3.3V Rail
- 5 ms 3 - Enable 1.8V Rail
- 5 ms 4 - Enable Core Rail
- 5 ms 5 - Enable 1.2V and 1.5V
- 5 ms 6 - Enable AVDD_OTG Rail
- 80 ms 7 - Deassert CPU_RESET#

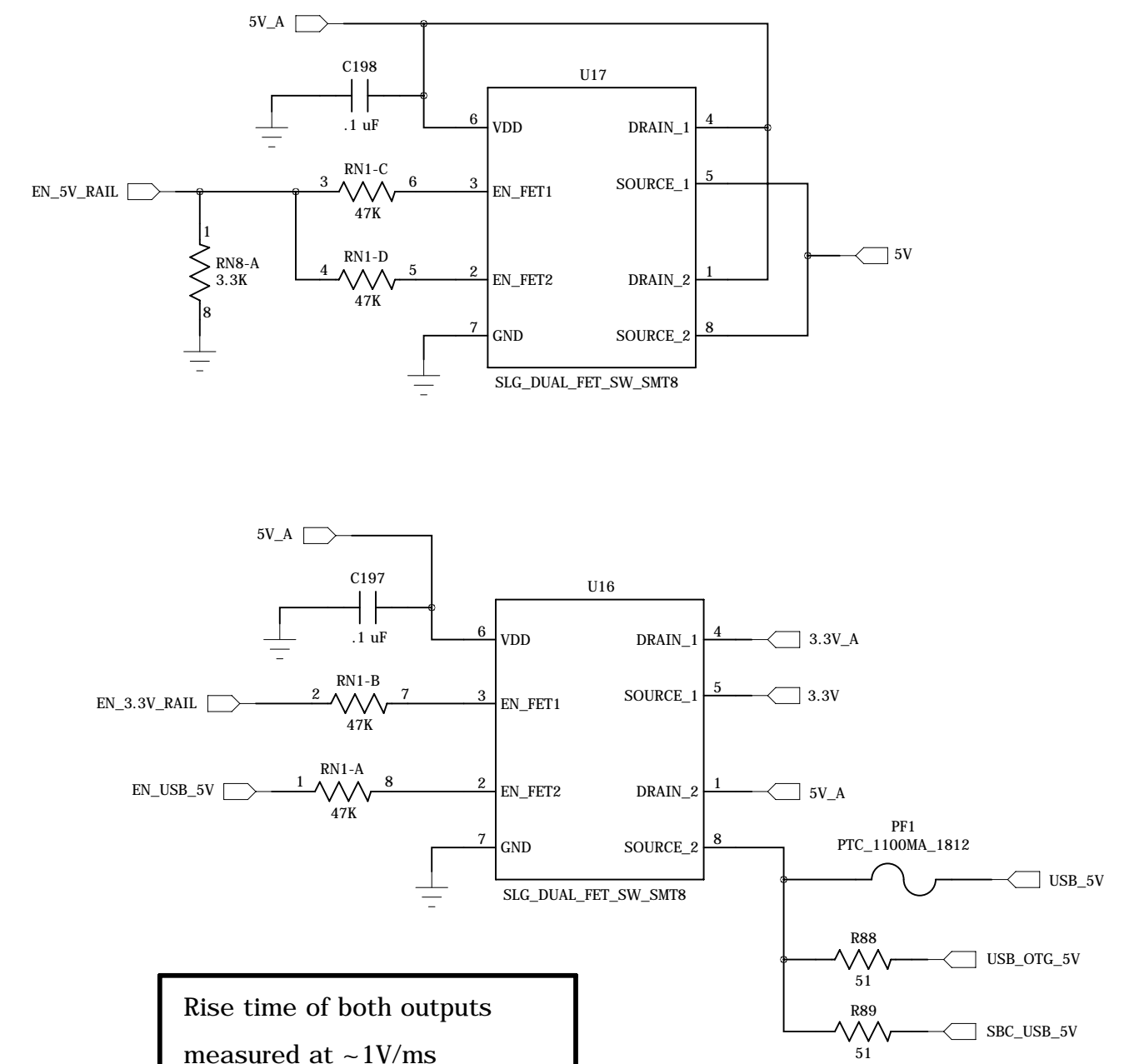
EN_SINK_1.2V is always complement of EN_1.2V_1.5V

If 5V_A < 4.0V, Deassert all Enables

USB Device Port



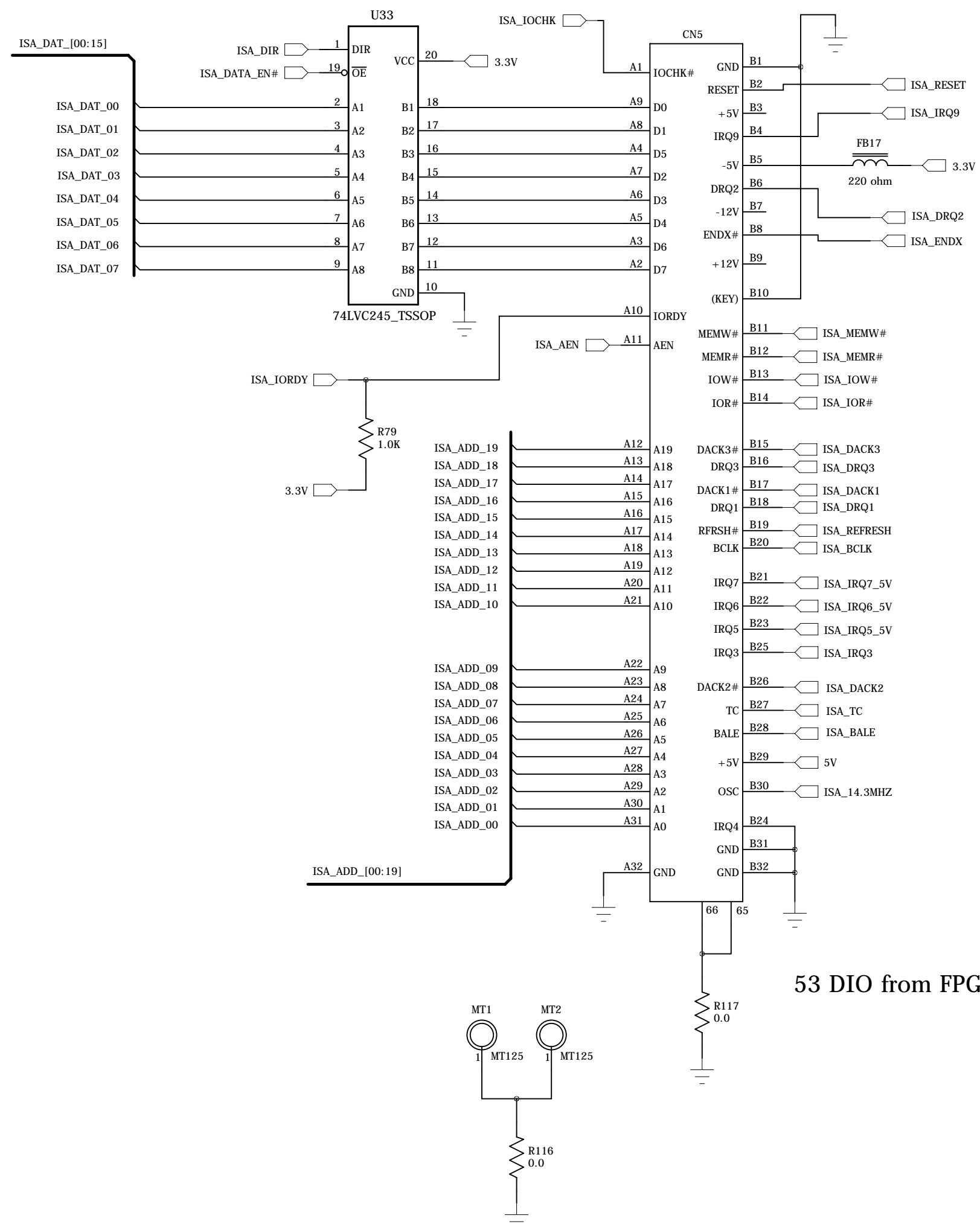
Switched Power



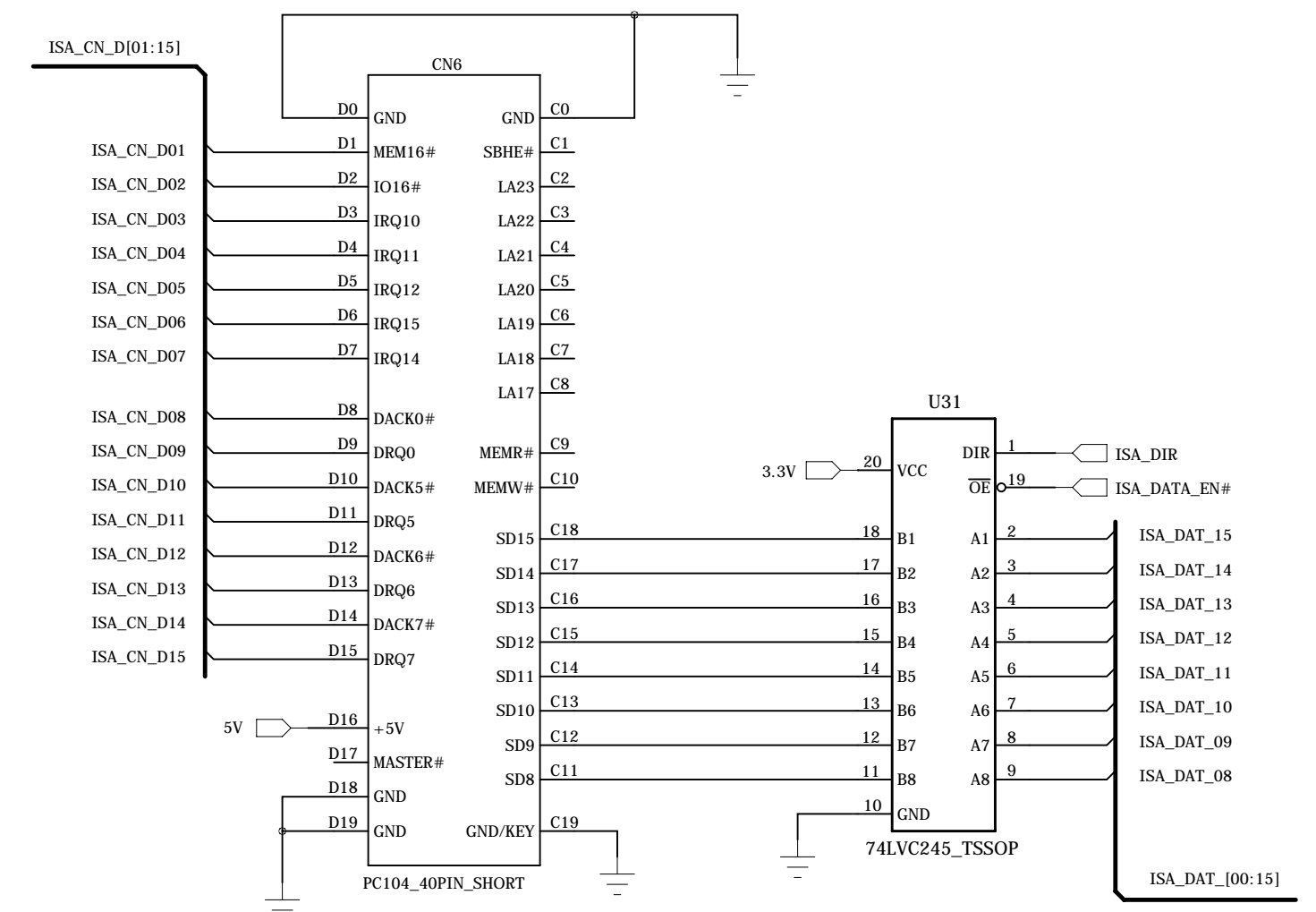
Rise time of both outputs measured at ~1V/ms

PC/104 Bus

PC/104 64-pin Connector



PC/104 40-pin Connector



Data lines and IRQ5-7
are all 5V tolerant

0 to +30V Input range

or

4-20 mA (3 channels)

Analog Inputs

