

# Comments:

Board can be powered from USB  
or by 8-28VDC, or by 24VAC

Cortex M0 is powered up first, then it controls MX286 start up

Cortex M0 does these functions:

- Controls MX286 power up sequence
- Controls MX286 Boot Strapping
- USB Device to Console conversion
- Controls Blue LED
- Can read Push Switch
- Measures Analog Vin value
- Reads SD\_BOOT Jumper
- Board ID

## Rev.P1 Problems:

## Serial Port Usage

UART0 = RS-232  
 UART1 = RS-232  
 UART2 = Modbus  
 UART3 = STC RS-485  
 UART4 = Blue or DC  
 Debug = Console/DC

DC = Daughter Card  
 STC = Screw Term. Conn.

# Notes:

- 1) Check Ethernet LEDs  
RAM\_1.8V rail turns on later than TS-7670  
Test 24VAC power
- 2) For Modbus 1042K baud operation - use DMA ?  
Serial Port RX DMA on MX286 says "must be multiples of 4 bytes"  
TX DMA does not say restricted to 4 byte multiples

### 3) BOM Warning:

R33, R34 and HD3 not pop  
 JP1 thru JP5 is 5x2 header = 15-3070-7  
 CAN ports are options  
 128MB and 256MB RAM sizes

UART2 and UART3 changed to SPI  
 when programming FPGA

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## I/O Diff from TS-7670

UART0\_RTS --> E2\_I2C\_CLK  
 UART0\_CTS --> E2\_I2C\_DAT  
 UART1\_CTS --> WIFI\_IRQ (1.8V)  
 DC\_DIO\_9 --> DISABLE\_TXEN2#  
 EN\_232\_TRANS = No Connect  
 EN\_ETH\_3.3V# = No Connect

GPS\_PPS\_OUT --> FPGA\_DONE  
 U3.R3 = FPGA\_RESET#  
 U3.U4 = FPGA\_SPI\_CS#  
 U3.T4 = FPGA\_IRQ  
 UART1\_RTS = FPGA\_SPARE\_0 (1.8V)  
 U3.U5 = FPGA\_SPARE\_1 (1.8V)  
 DC\_DIO\_8 = FPGA\_SPARE\_2 (1.8V)

Changed VIN A/D scaling !

## CAN Option

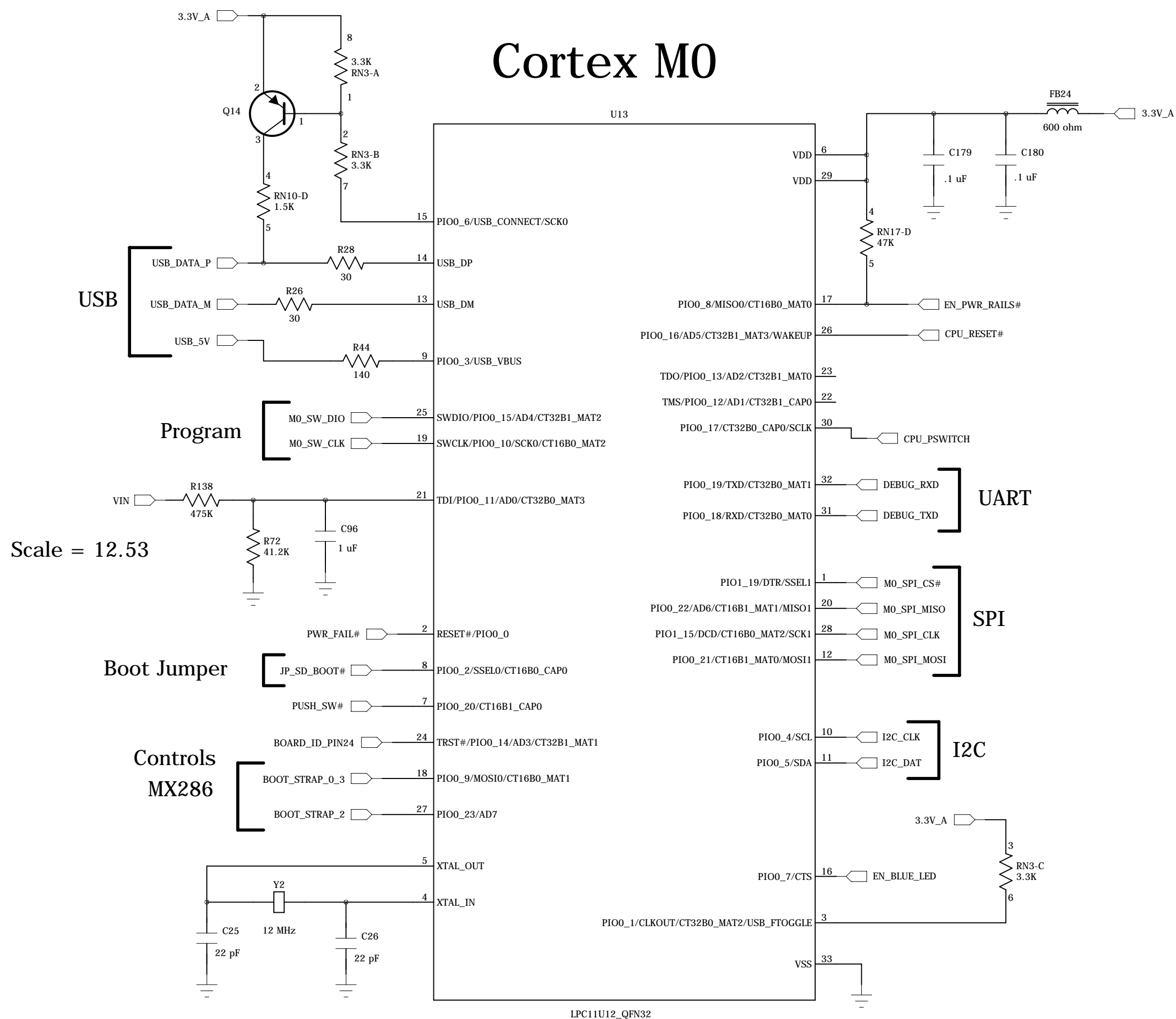
U25, U26 and TVS16

## Warning: 1.8V Levels

- SD2 signals
- WIFI\_IRQ
- FPGA\_SPARE\_0
- FPGA\_SPARE\_1
- FPGA\_SPARE\_2

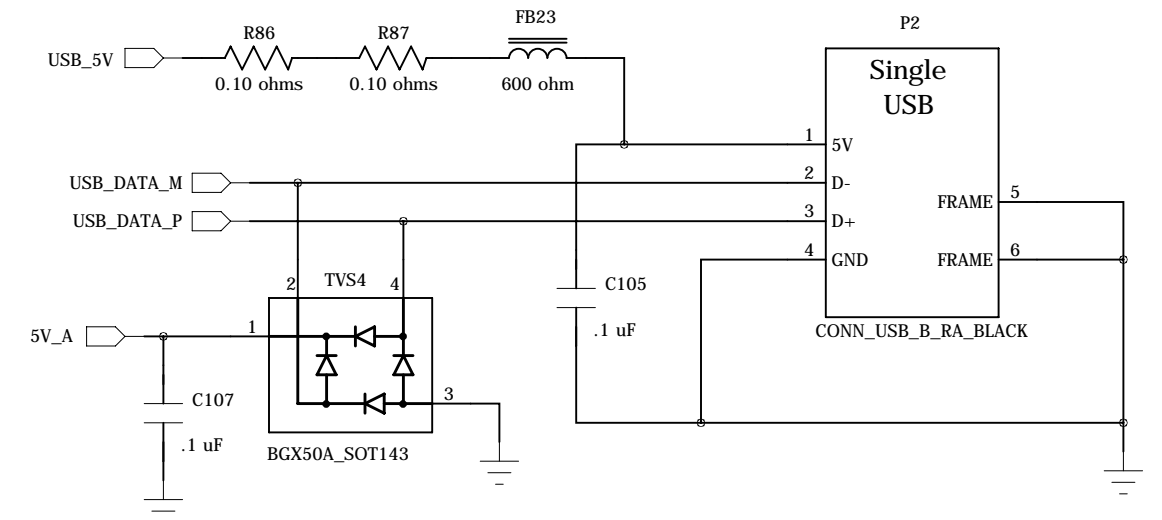
Technologic Systems	Date	April 21, 2014
Title: TS-7680 Documentation		
Rev: P1	Designer	Sheet 1 of 18

# USB Device Port and Cortex M0

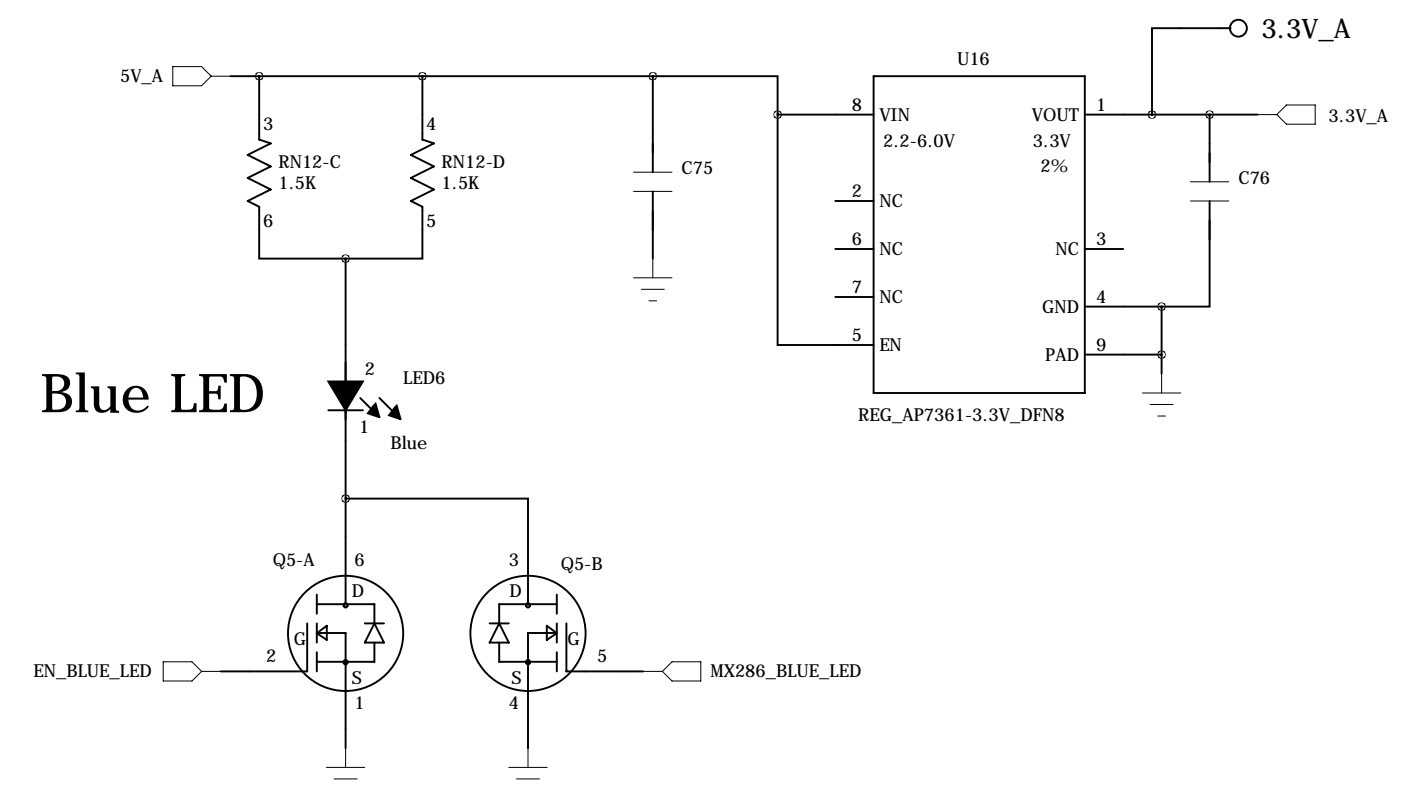


Pins 2 and 3 must be high at PU

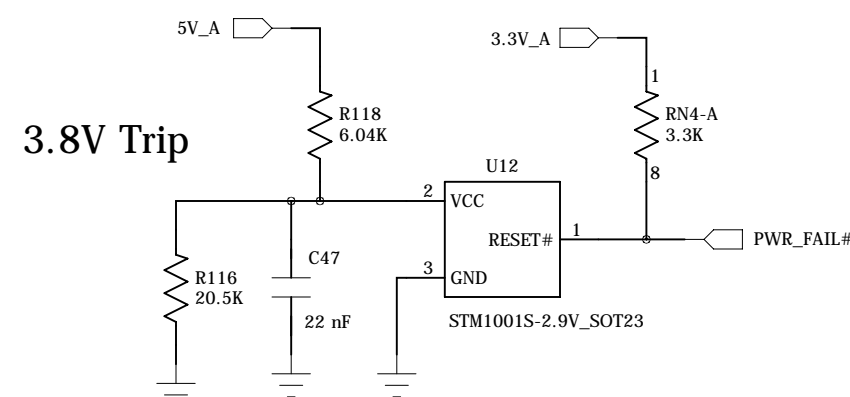
## USB Device Port



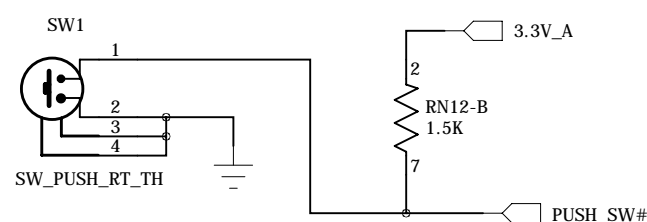
## 3.3V Reg. for M0



## Brown out Detect

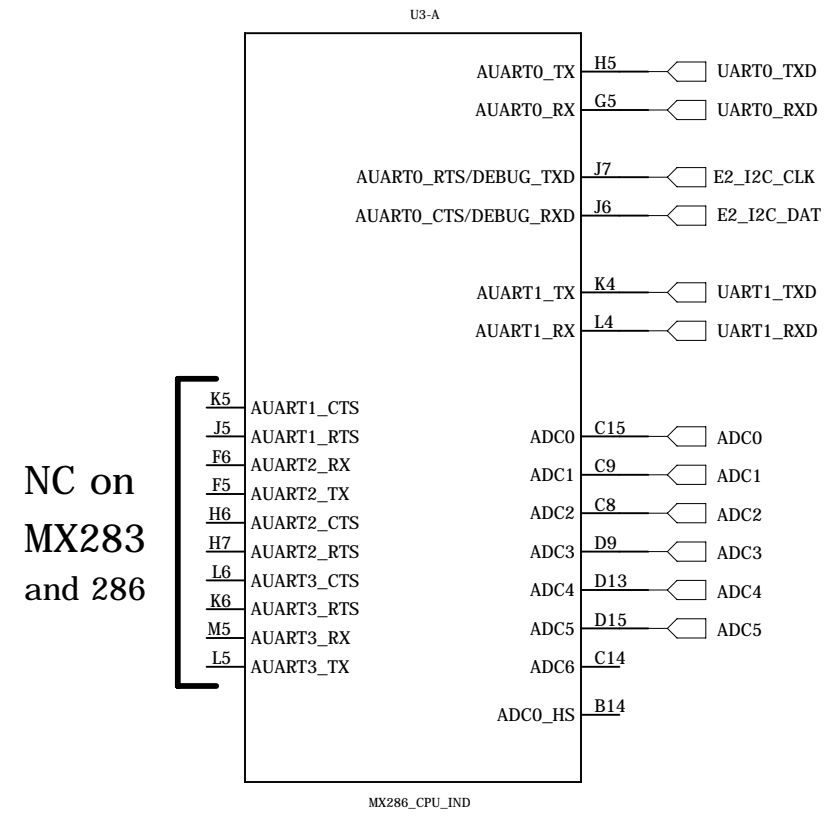


## Push Switch

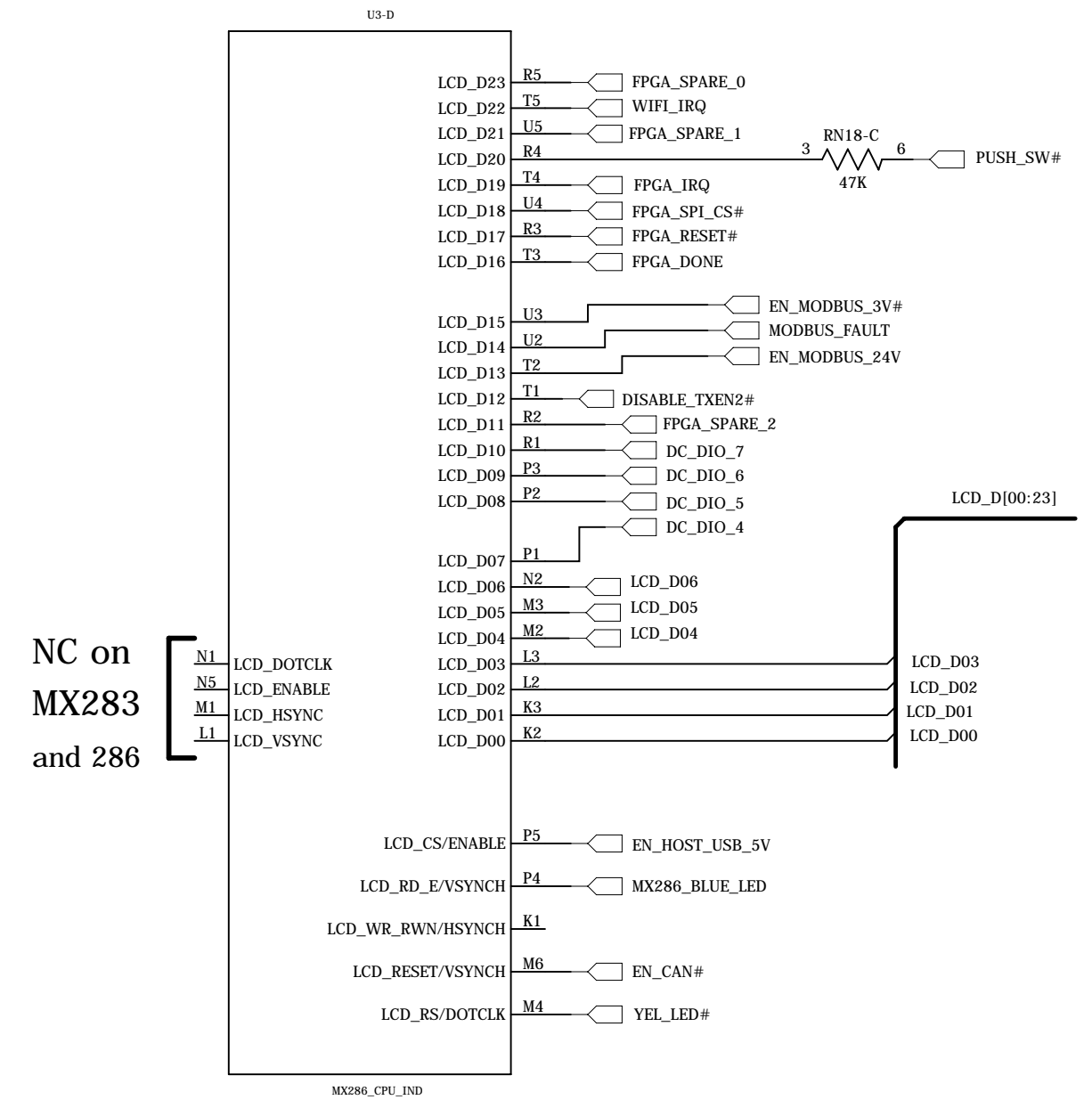


# MX286 ARM9 CPU

## UARTs, ADC

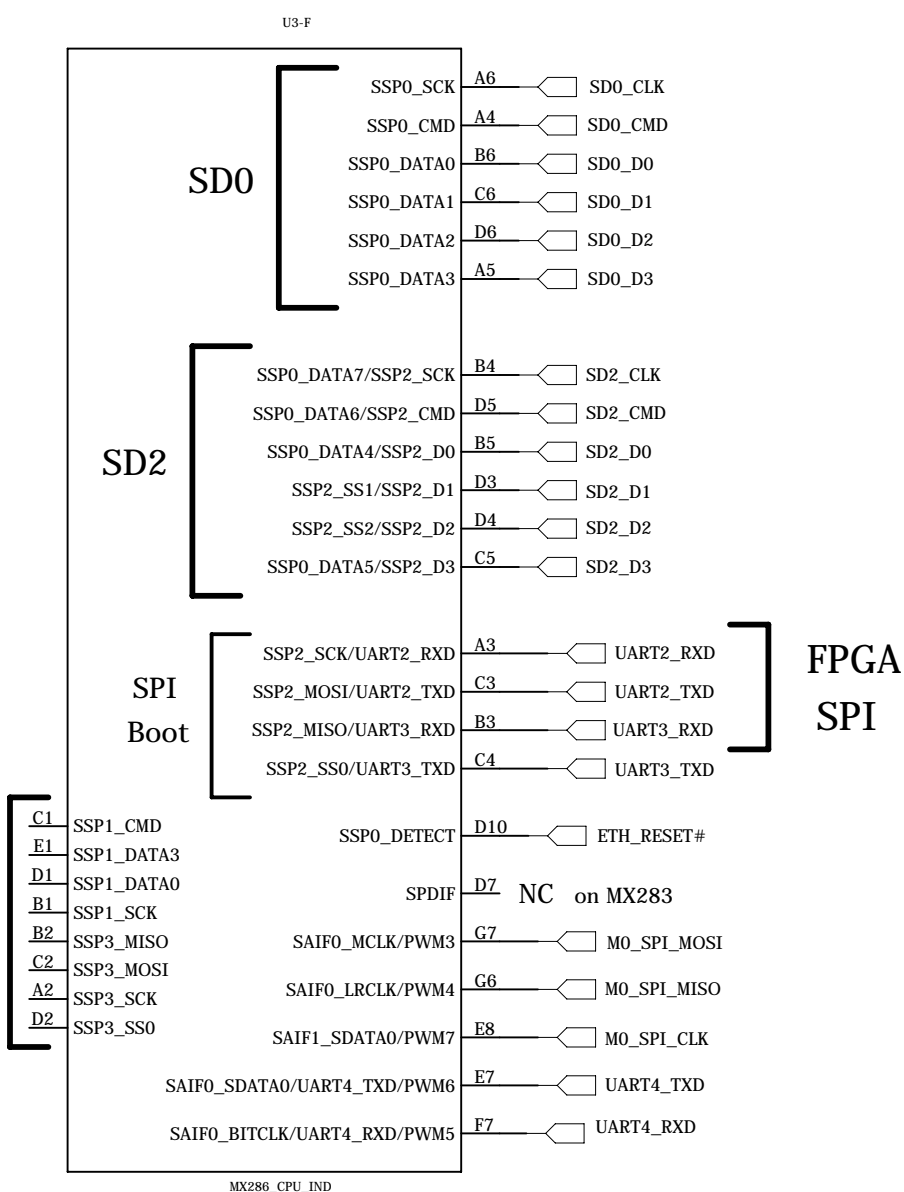


## LCD



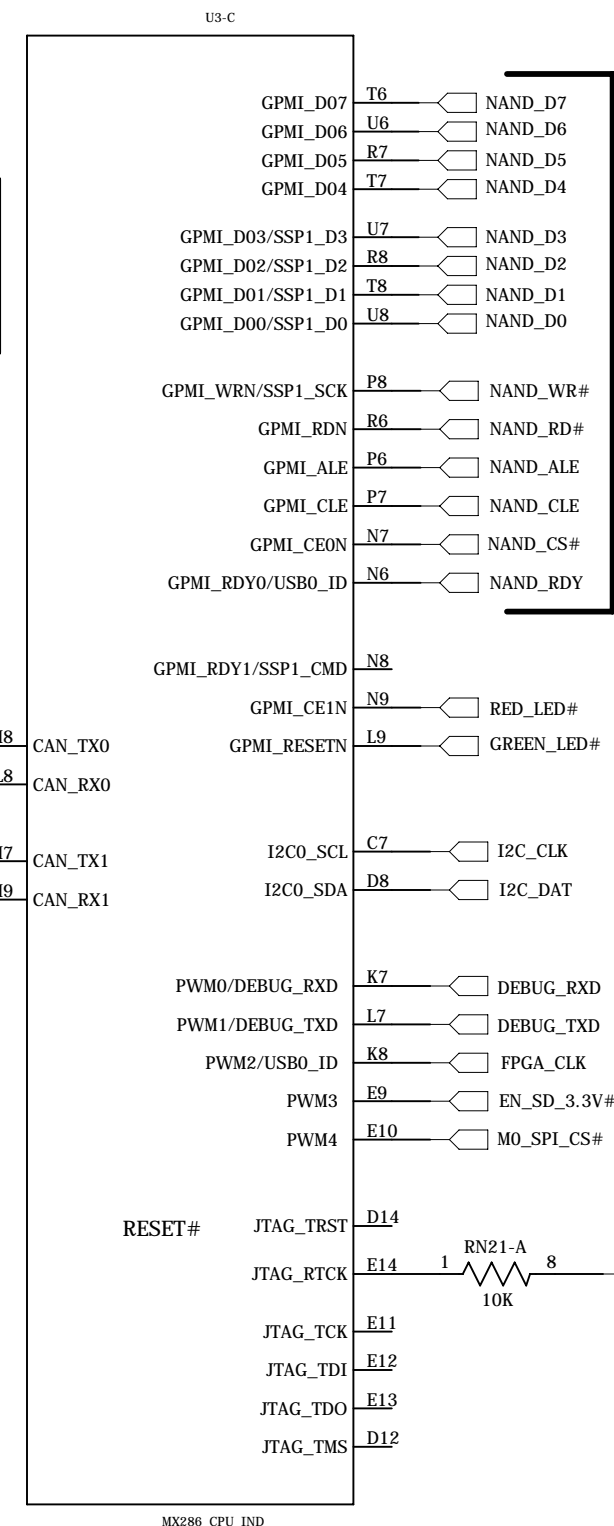
## NAND, PWM JTAG, I2C

## Audio SD Card SPI Boot



SPI  
SCK = CLK  
CMD = MOSI  
DO = MISO  
D3 = CS#

MX286 adds  
4 CAN signals  
and ball D7



NAND Interface

LCD\_00 thru LCD\_04  
Control Boot Source

LCD\_05 and 06 bias low  
LCD\_RS biased high  
LCD\_RS low = use OTP  
See: EVK schematic, Page 15

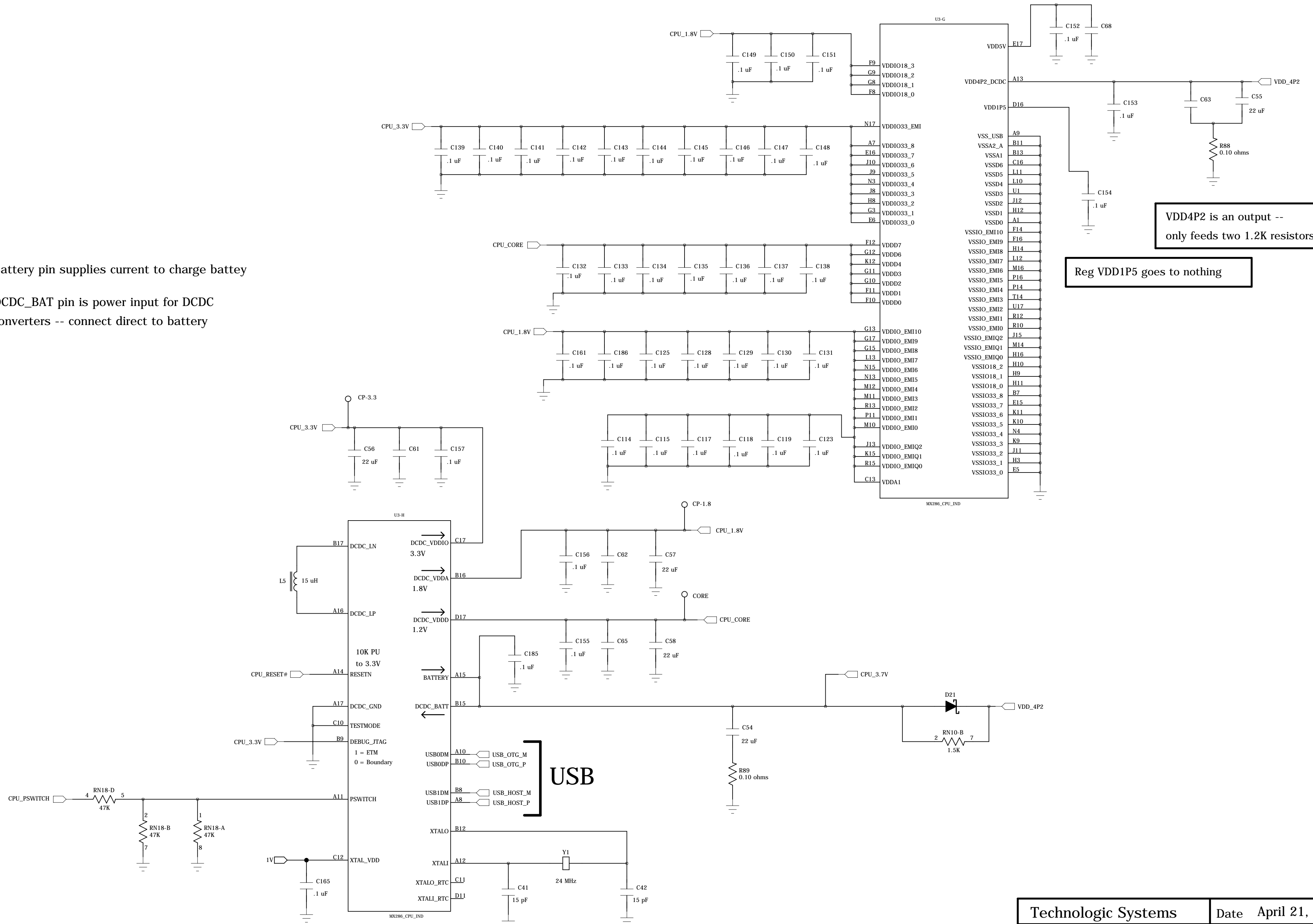
F3 is EVK ETH\_RESET#  
F5, F6 are EVK USB\_PWR\_EN  
E1 is EVK Eth\_PWR\_EN  
C7 and D8 = EVK I2C  
J5 is EVK USB\_0\_ID  
K8 is EVK LCD PWM  
K7 and L7 are EVK console

E10 is EVK SD1\_PWR\_EN  
E9 is SD0 PWR\_EN on both  
EVK and Green schematics

PWM outputs can be 24 MHz  
divided by 16-bit integer  
Allows clock 12MHz and lower

Battery pin supplies current to charge battery

DCDC\_BAT pin is power input for DCDC converters -- connect direct to battery



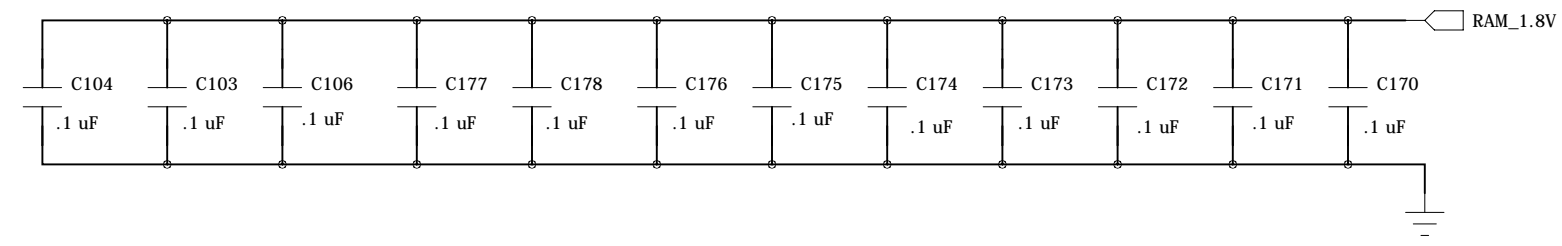
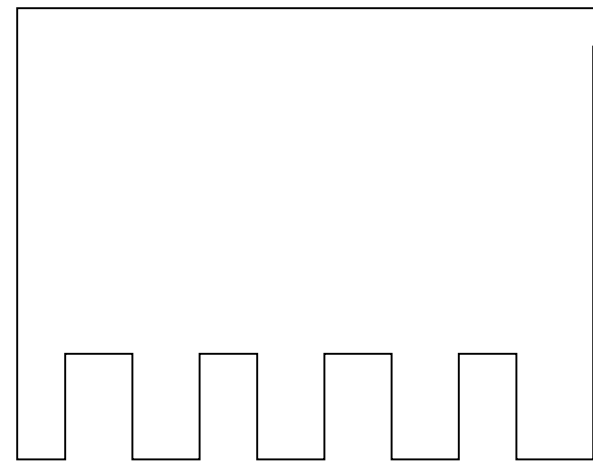
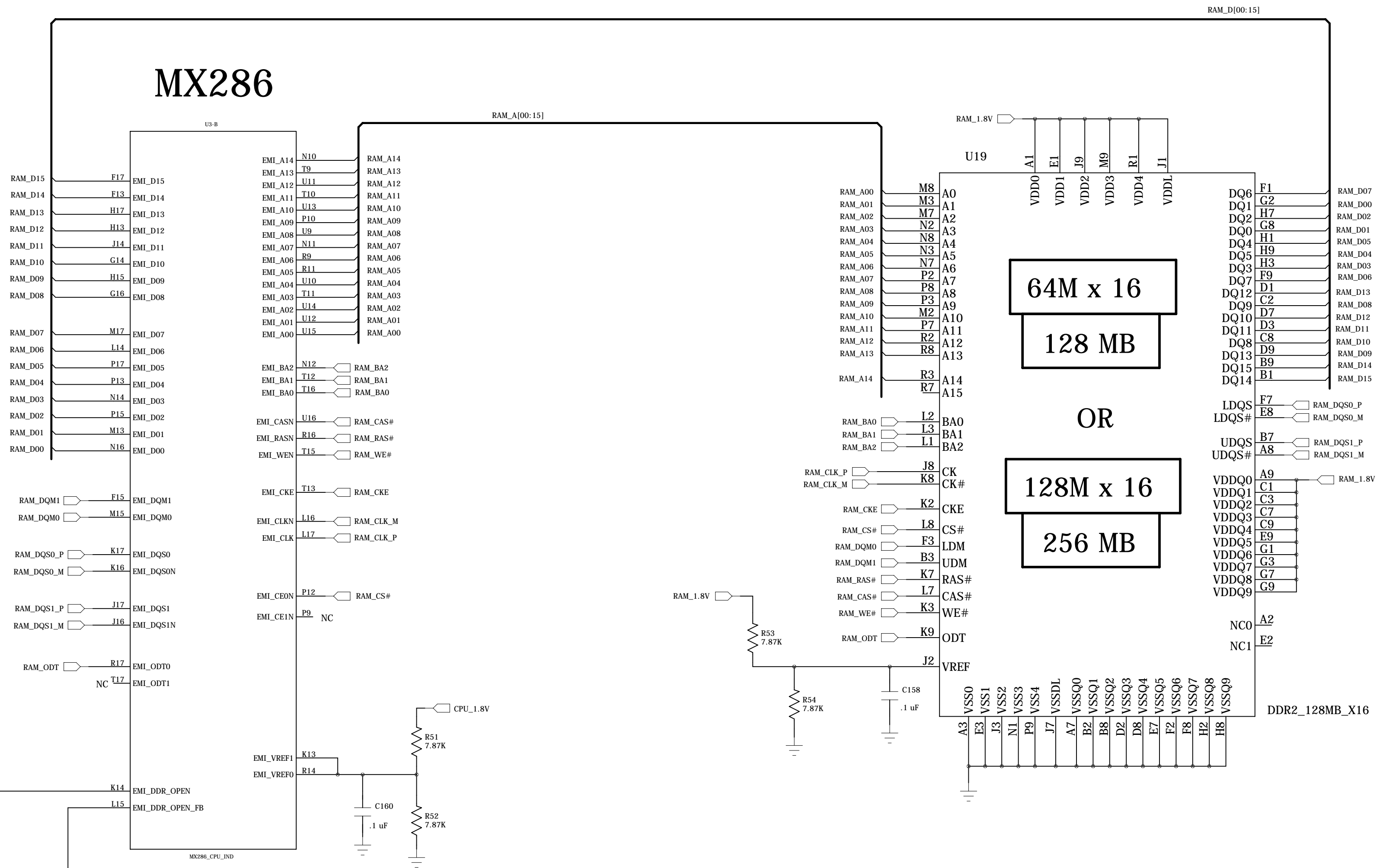
VDD4P2 is an output -- only feeds two 1.2K resistors

Reg VDD1P5 goes to nothing

PSWITCH can be driven to 3.3V if a series 10K res is used

Technologic Systems	Date April 21, 2014
Title: TS-7680 MX286 CPU Power	
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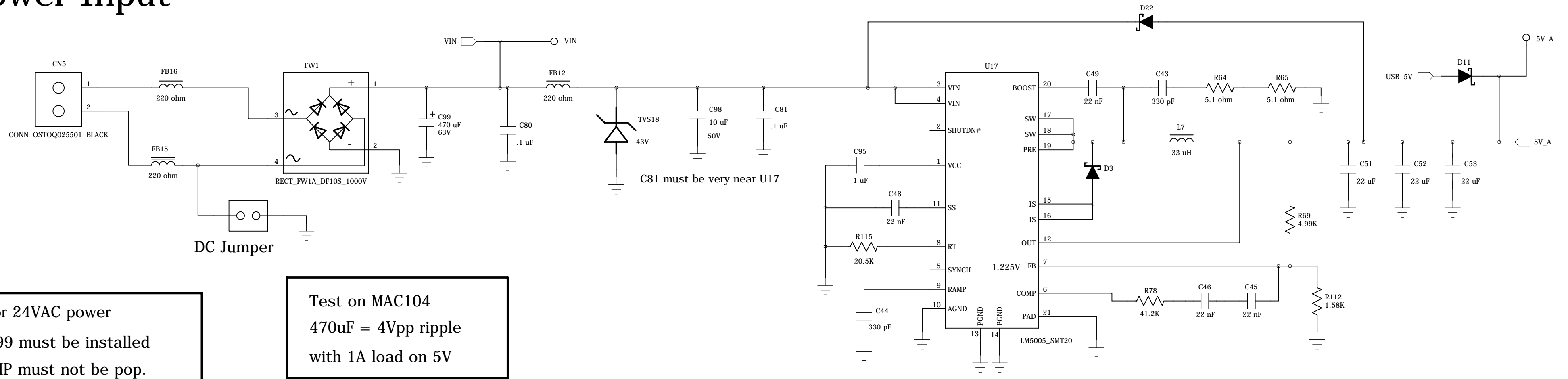
# DDR2 SDRAM (128 or 256 MByte)



# 5V Power Supply (2000 mA)

D11 allows USB to power MX286  
 This will only work if 3.7V  
 Reg (U7) is powering MX286

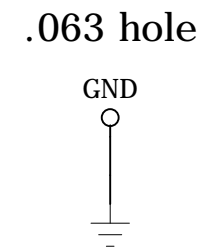
## 8-28 VDC Power Input



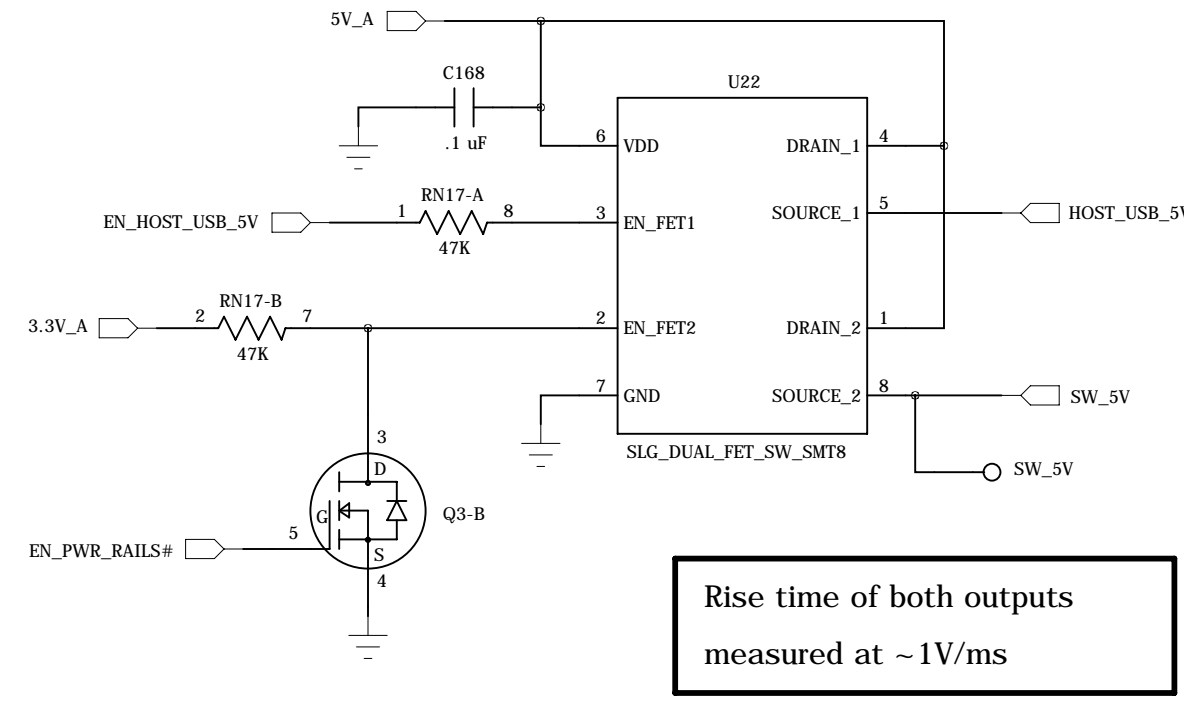
For 24VAC power  
 C99 must be installed  
 JMP must not be pop.

Test on MAC104  
 470uF = 4Vpp ripple  
 with 1A load on 5V

C81 must be very near U17

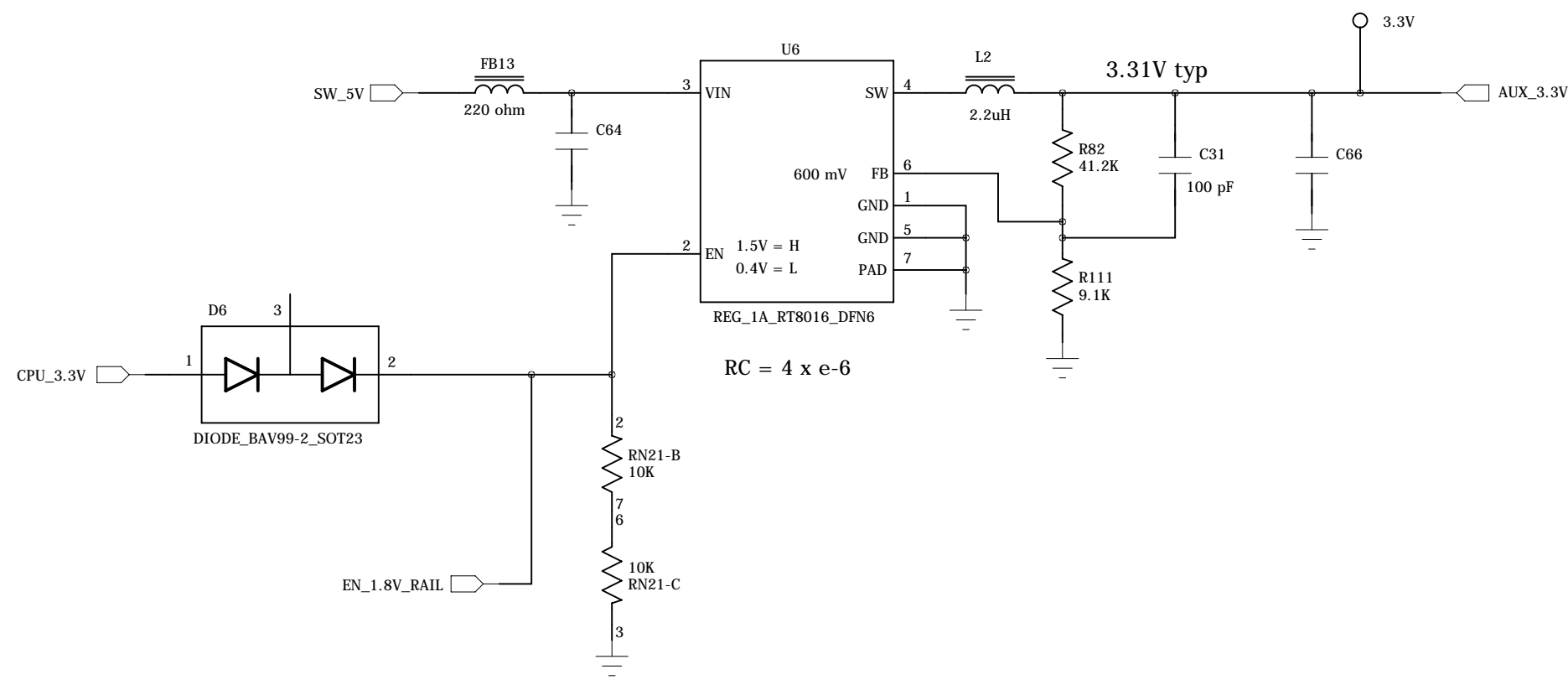


## USB and MX286 Switched Power



Rise time of both outputs  
 measured at ~1V/ms

# Aux. 3.3V Reg

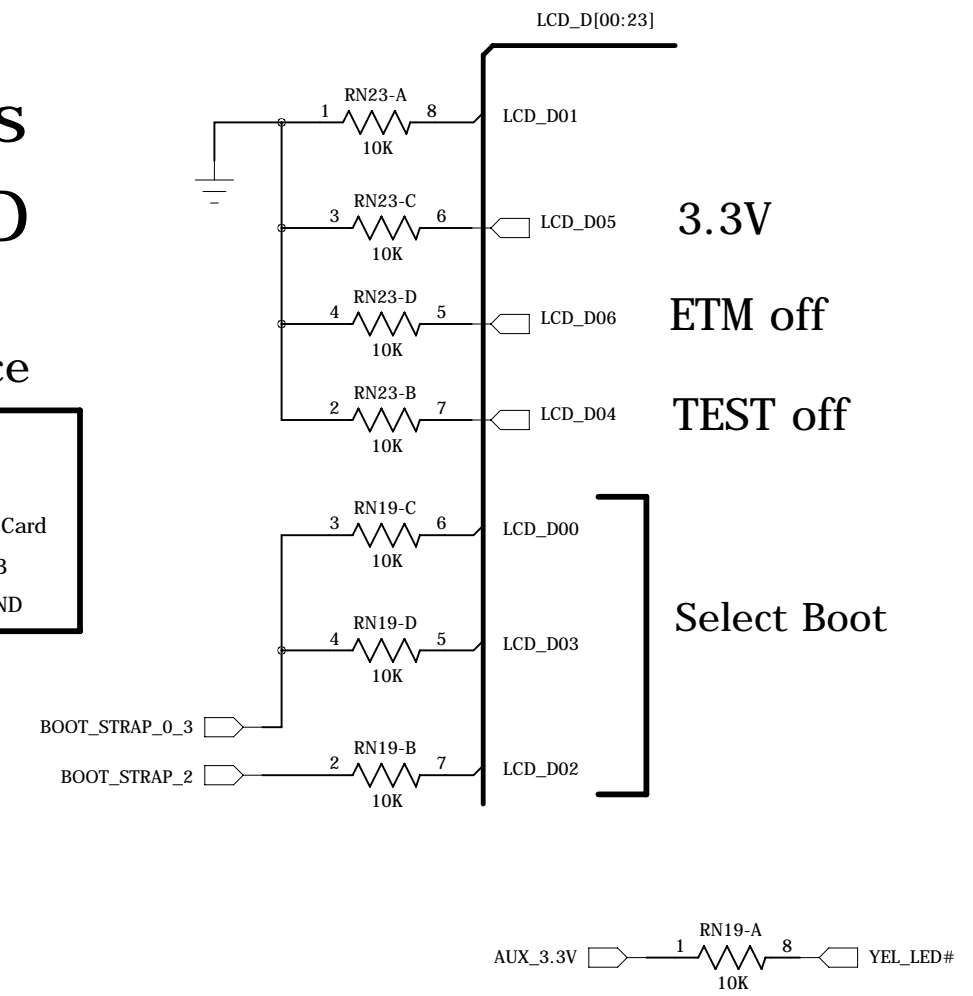


# Boot Strap Bias Res.

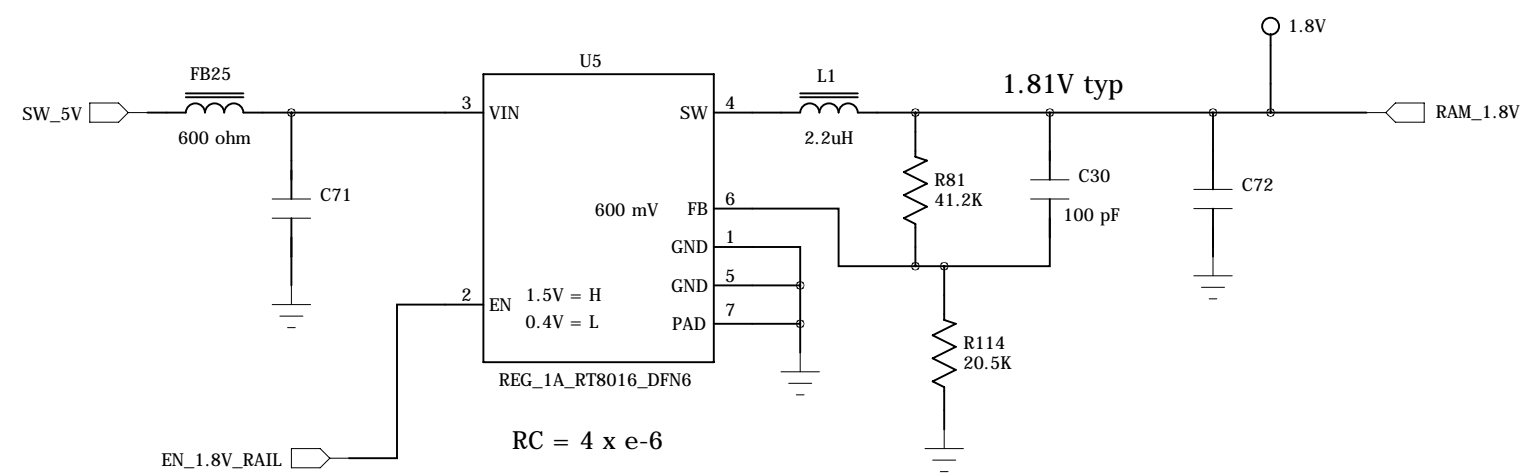
Defaults to NAND

Boot Source

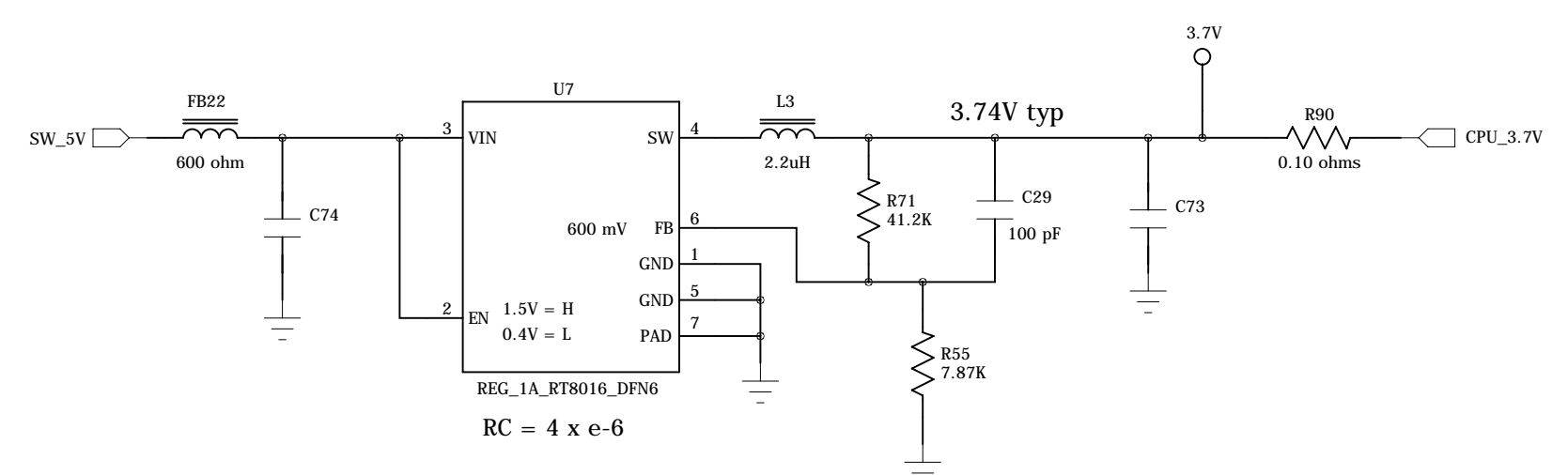
LCD_3	LCD_0	
0	0	SPI
1	0	SD Card
0	0	USB
0	1	NAND



# RAM 1.8V Reg



# CPU BATT 3.7V



This Reg only required for extra low power mode

FB7 not installed when this reg. is used

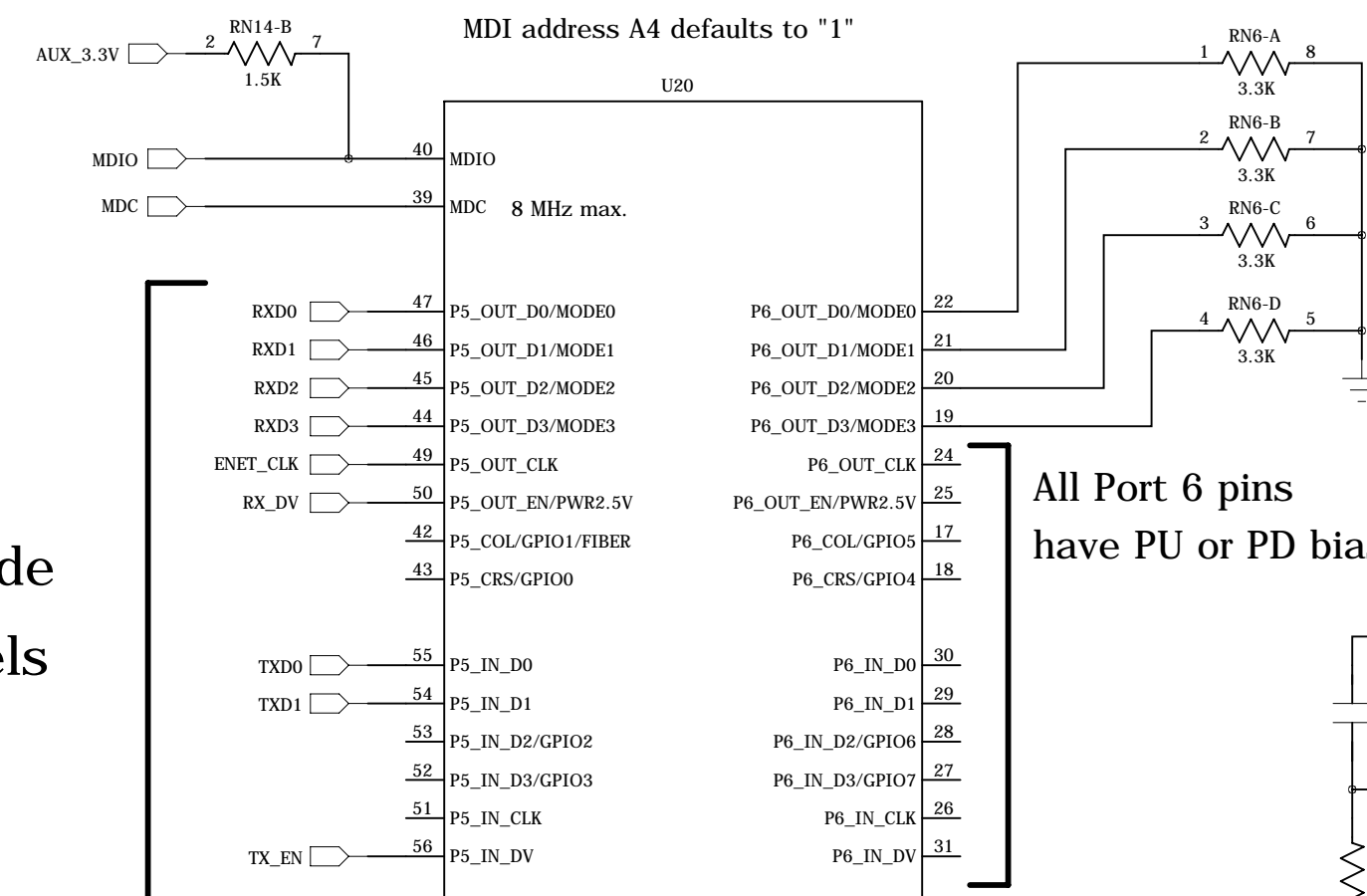
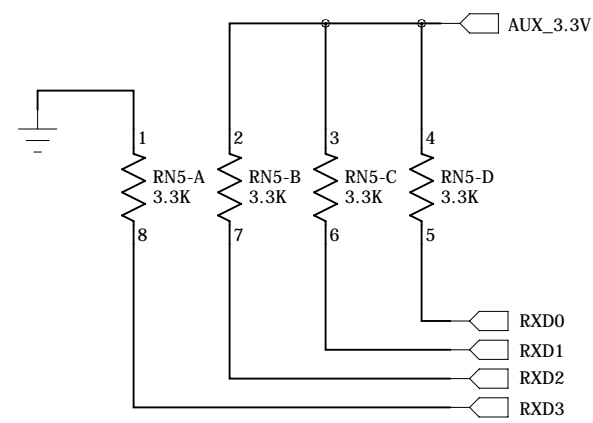
Requires a positive pulse on PSWITCH

# 10/100 Ethernet 4-Port Switch

Total 88E6020 100 Mbit  
 Current Drain includes  
 2 Ports with Mag CT  
 3.3V Rail = 20 mA  
 1.8V Rail = 80 mA  
 1.2V Rail = 62 mA  
 Power Down mode  
 42 mA on 1.2V rail  
 0 mA on other rails

Pull-downs default P6  
 to port disabled mode

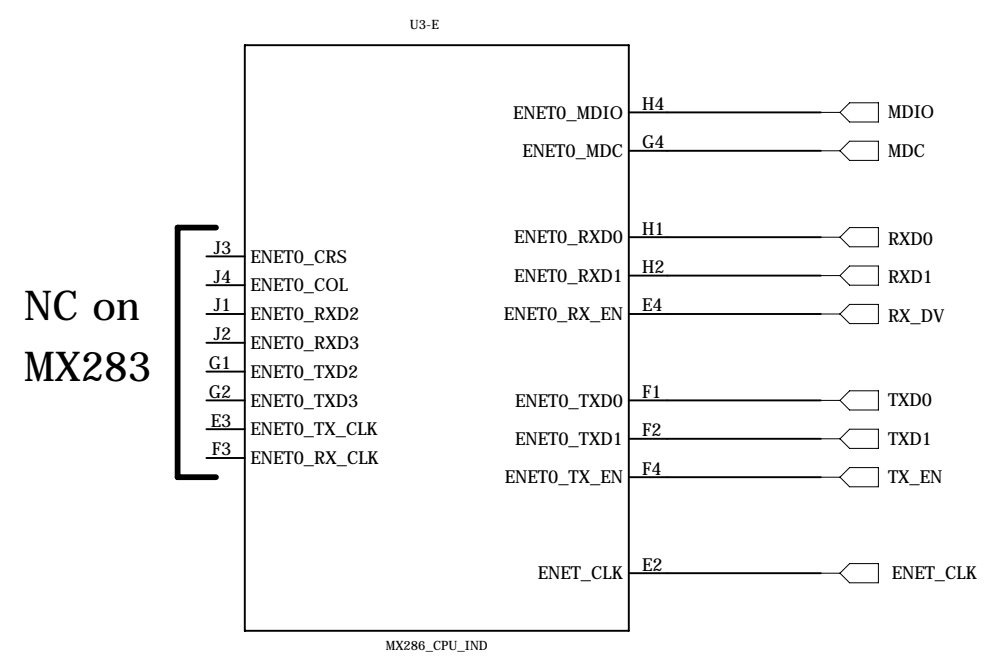
"0111" = RMII MAC mode



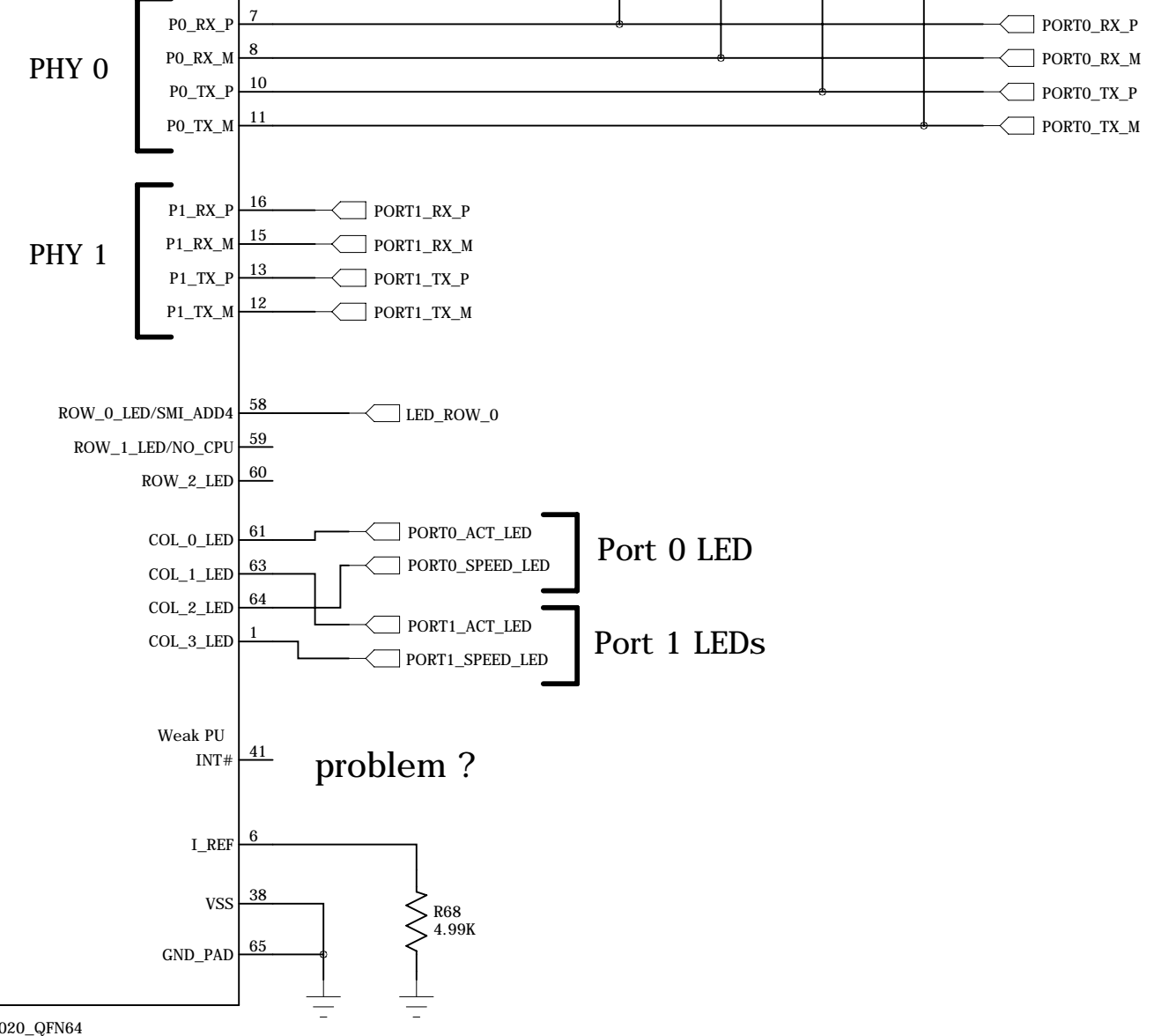
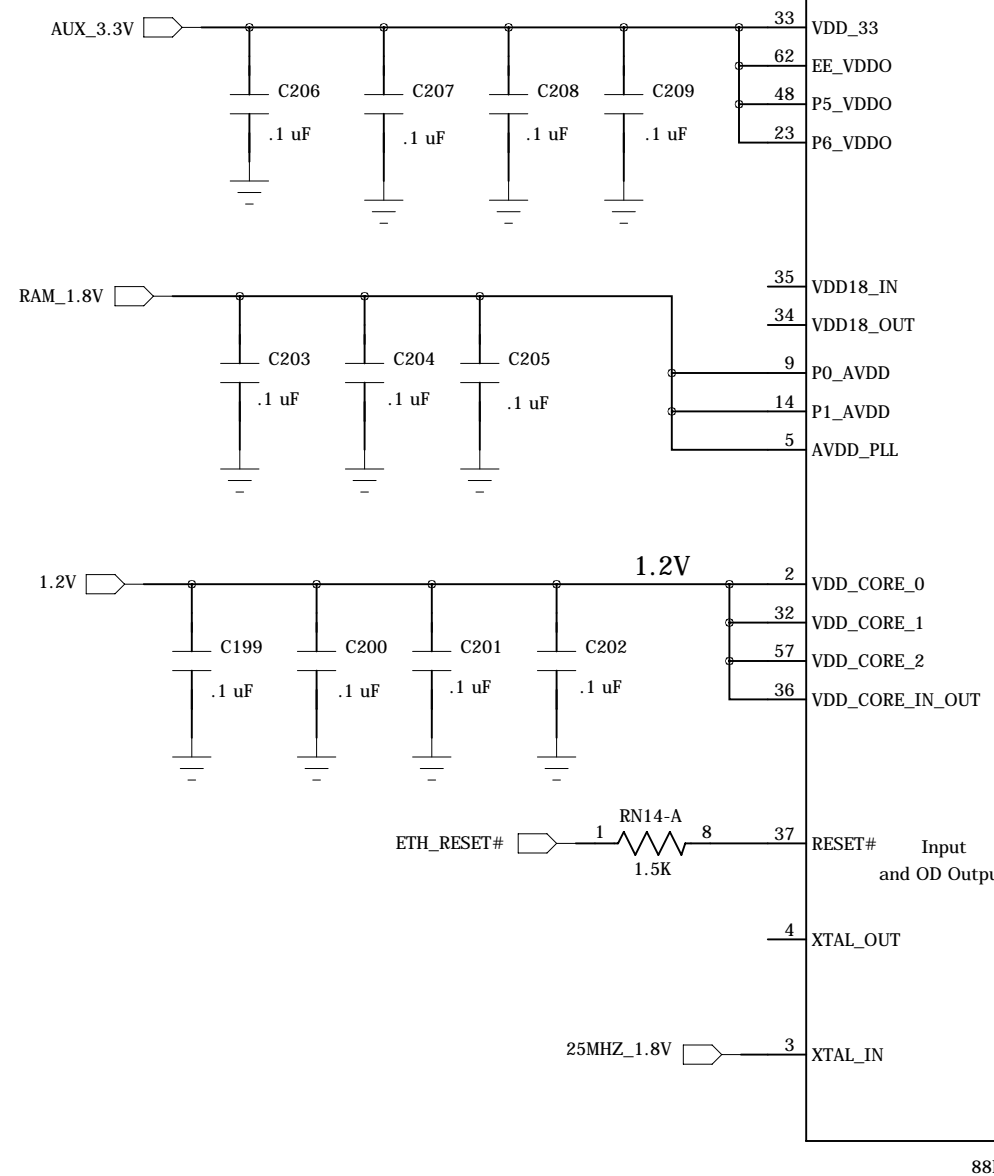
Strapped for  
 RMII MAC mode  
 with 3.3V Levels

All Port 6 pins  
 have PU or PD bias

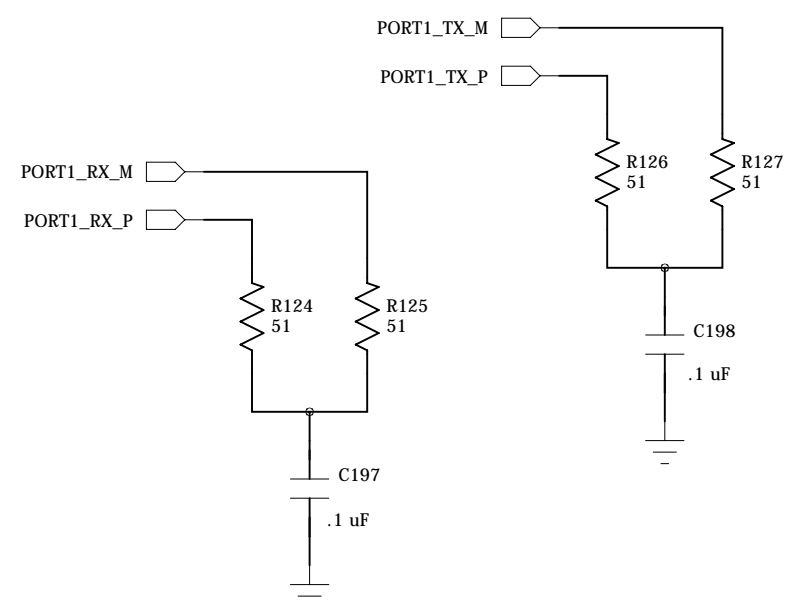
## MX283



NC on  
 MX283



Requires Reset# asserted  
 for 10 ms after power

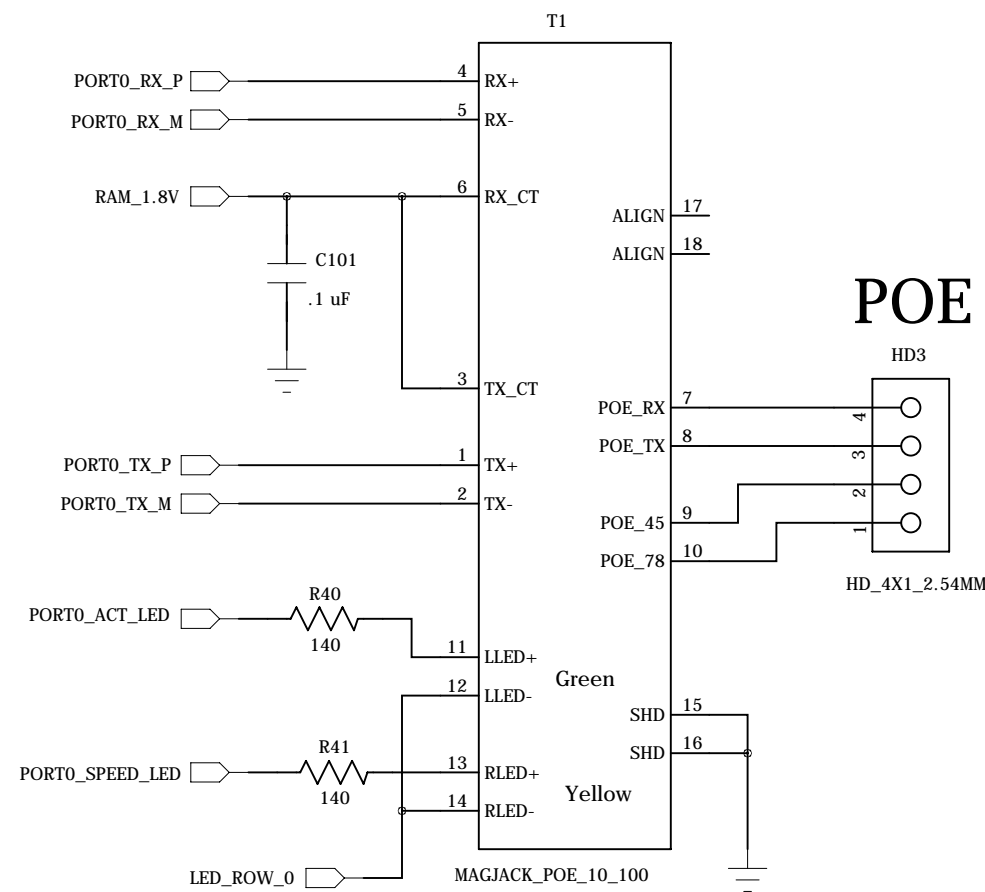


Auto MDIX is supported  
 Polarity Correction also supported

Technologic Systems	Date April 21, 2014
Title: TS-7680 Ethernet Switch	
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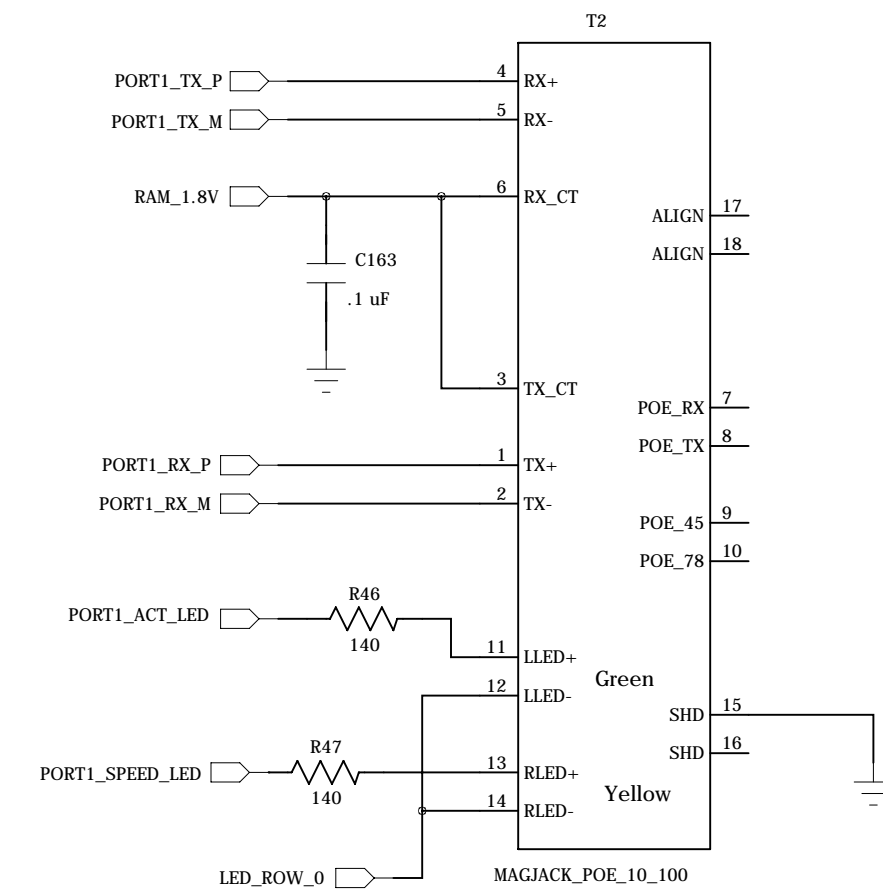


## Port #0 10/100 MagJack



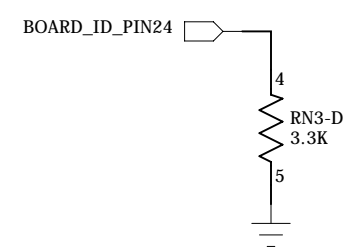
Test LEDs on Prototype

## Port #1 10/100 MagJack



Pin 16 deleted from GND  
for layout purposes

## Board ID



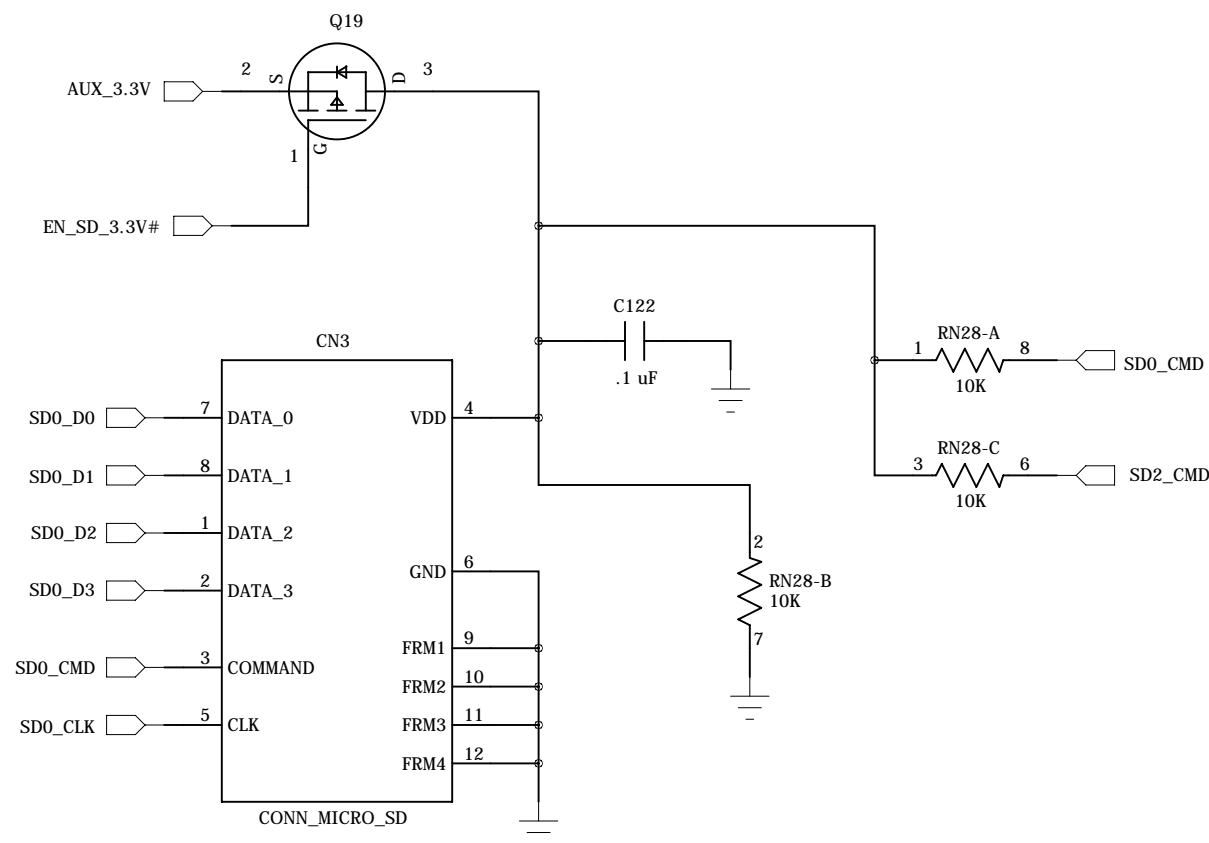
## M0 Board ID

Pin 22	Pin 23	Pin 24	
1	x	1	TS-7670
1	1	0	TS-7680

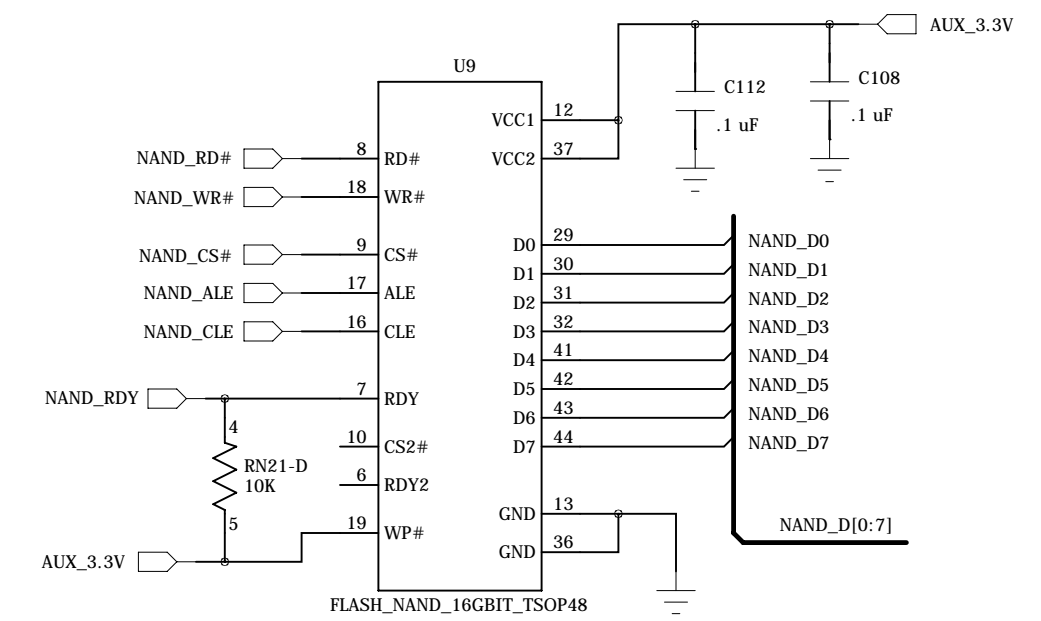
Assumes weak PU on these 3 pins

# Flash Memory

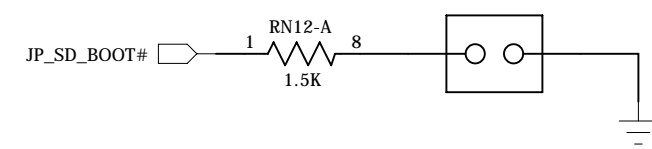
## Micro SD Card Socket



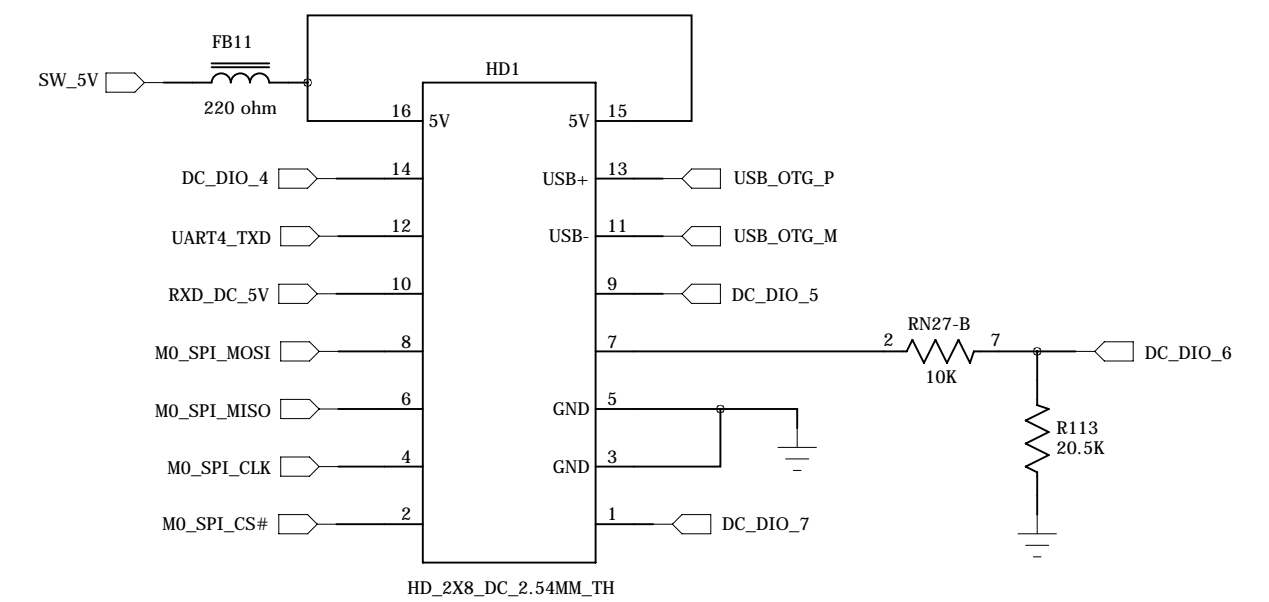
## NAND Flash



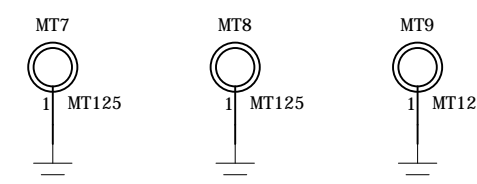
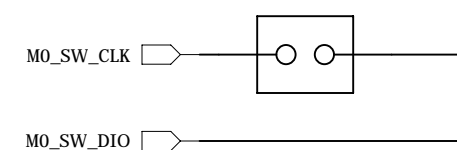
## SD Boot Jumper



## Daughter Card Interface



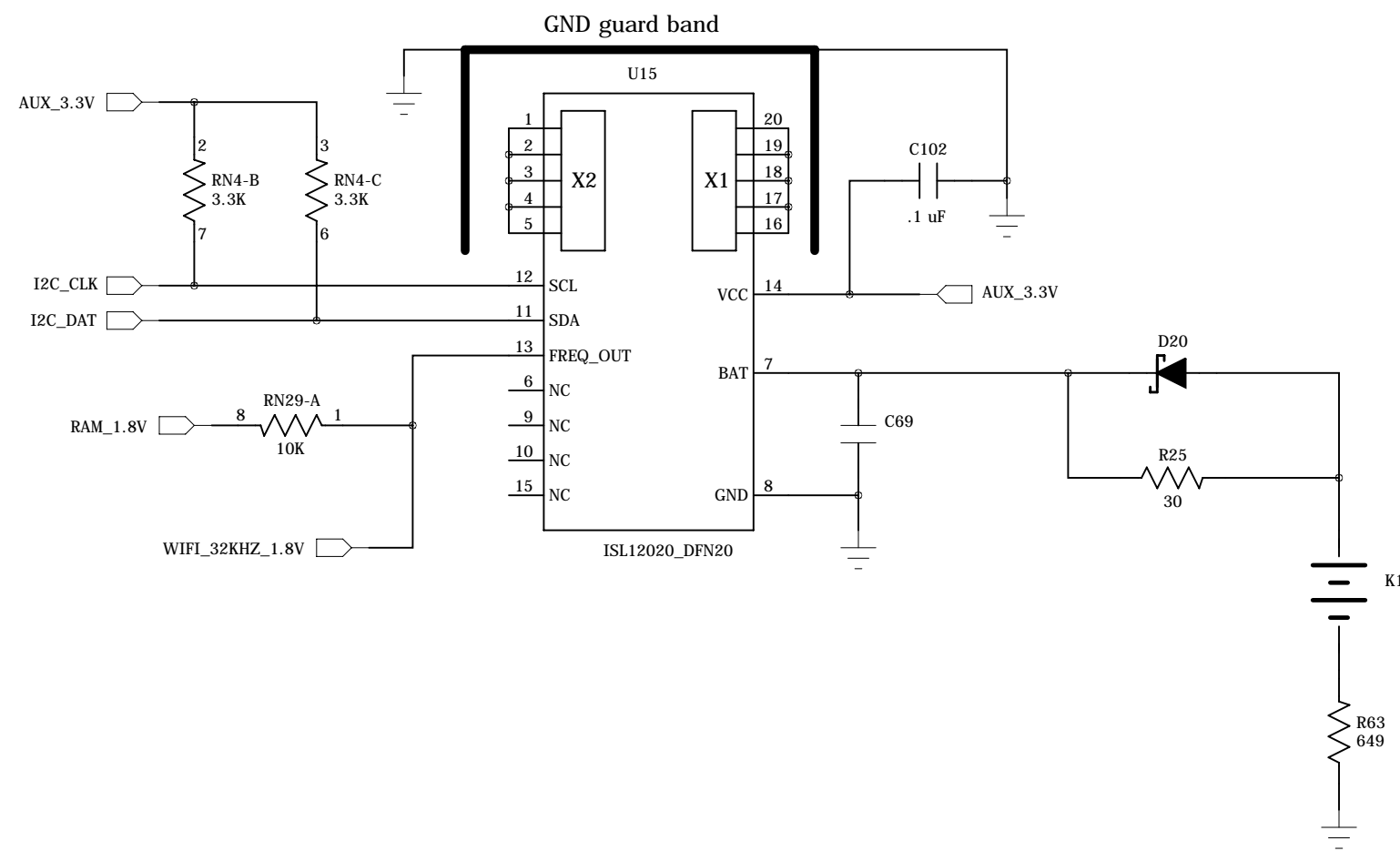
## M0 Program Header



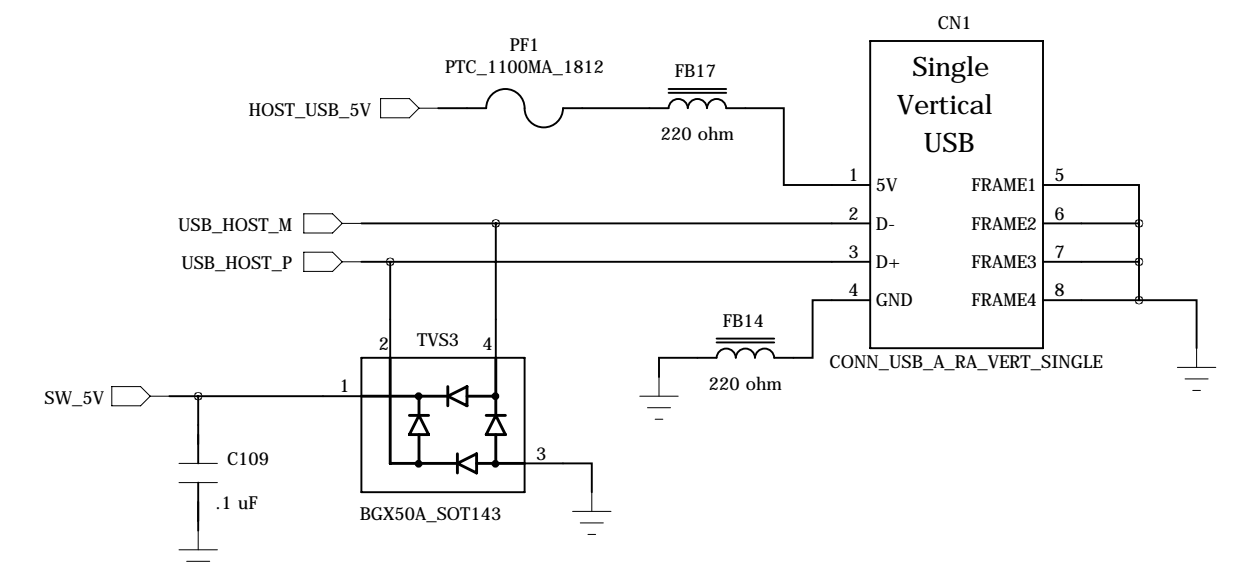
Technologic Systems	Date April 21, 2014
Title: TS-7680 NAND and SD Card	
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# RTC and Host USB

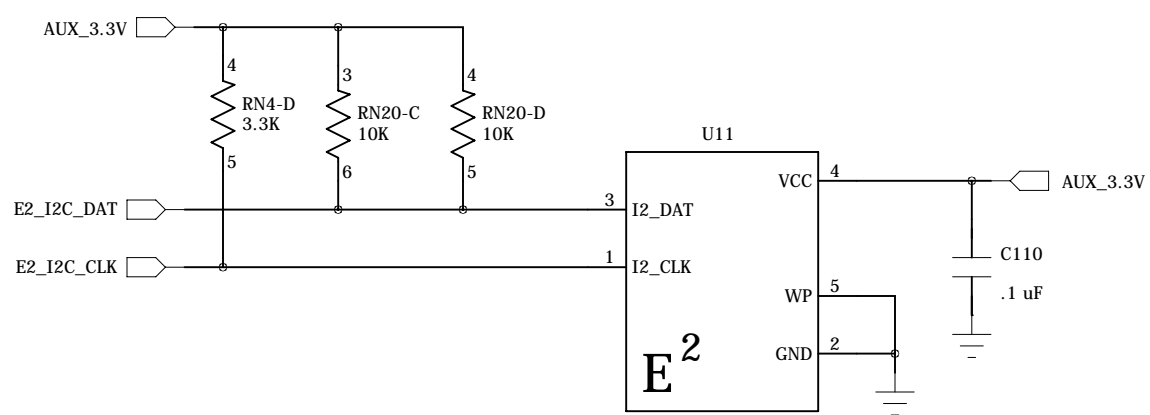
## RTC and Temp. Sensor



## External Host USB Port



## EEPROM 1 Kbyte

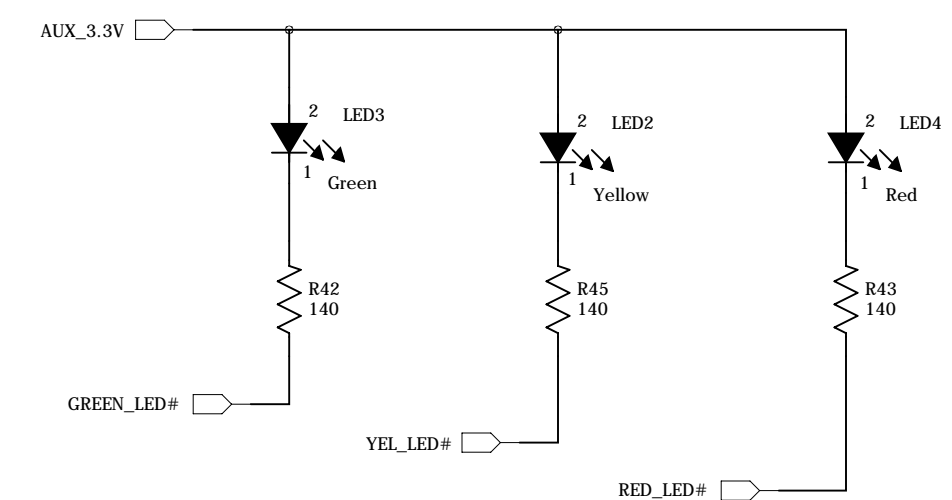


For Calibration Values

## Warning

There is a I2C address conflict  
between the RTC RAM and the EEPROM  
EEPROM must use separate I2C bus

## SMT RA LEDs



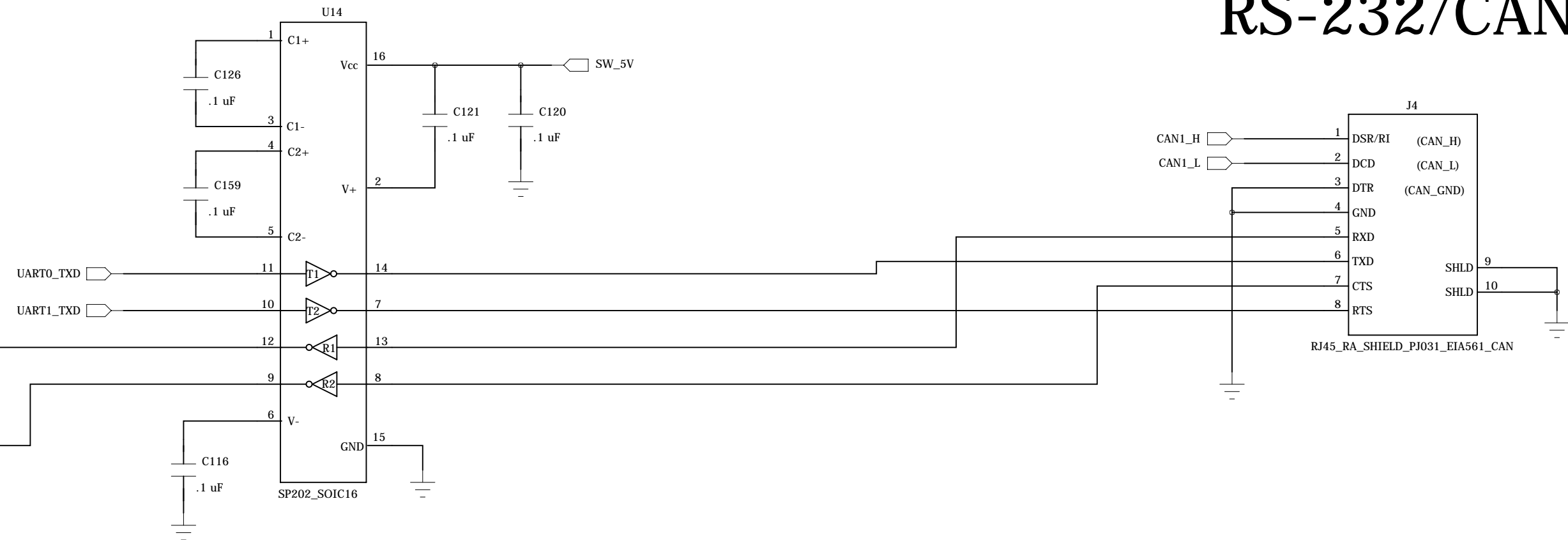
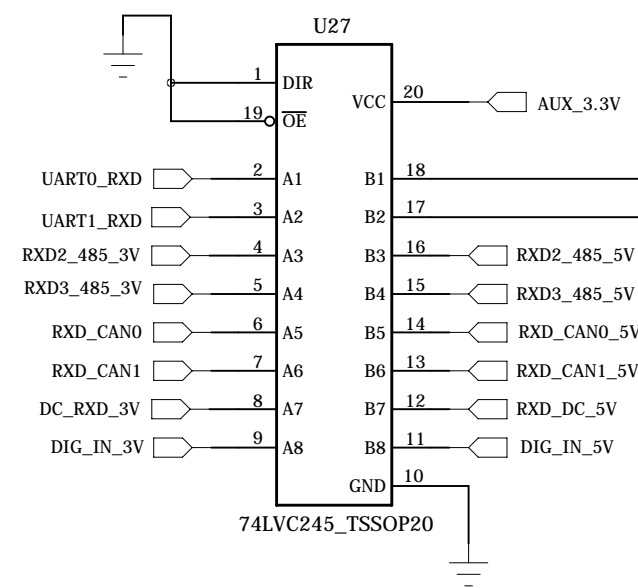
# RS-232 Ports and Daughter Card Headers

## RS-232 Transceiver

## RS-232/CAN

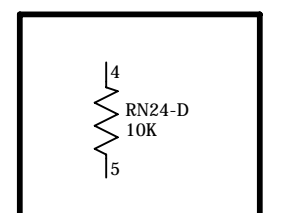
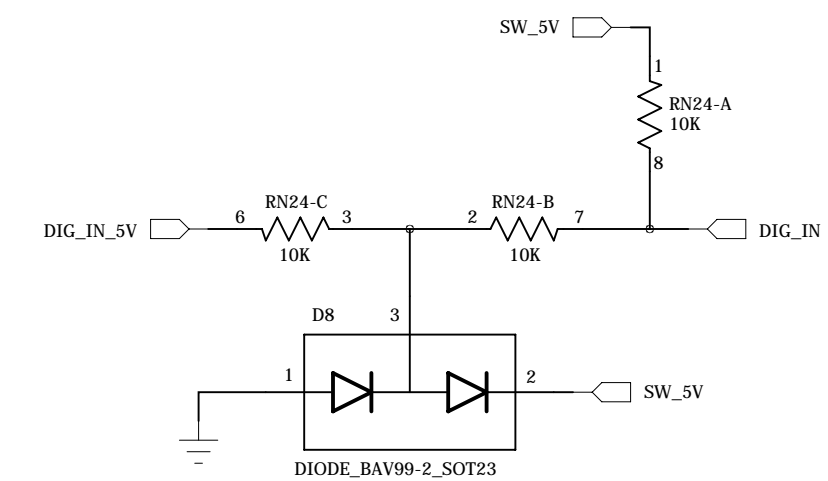
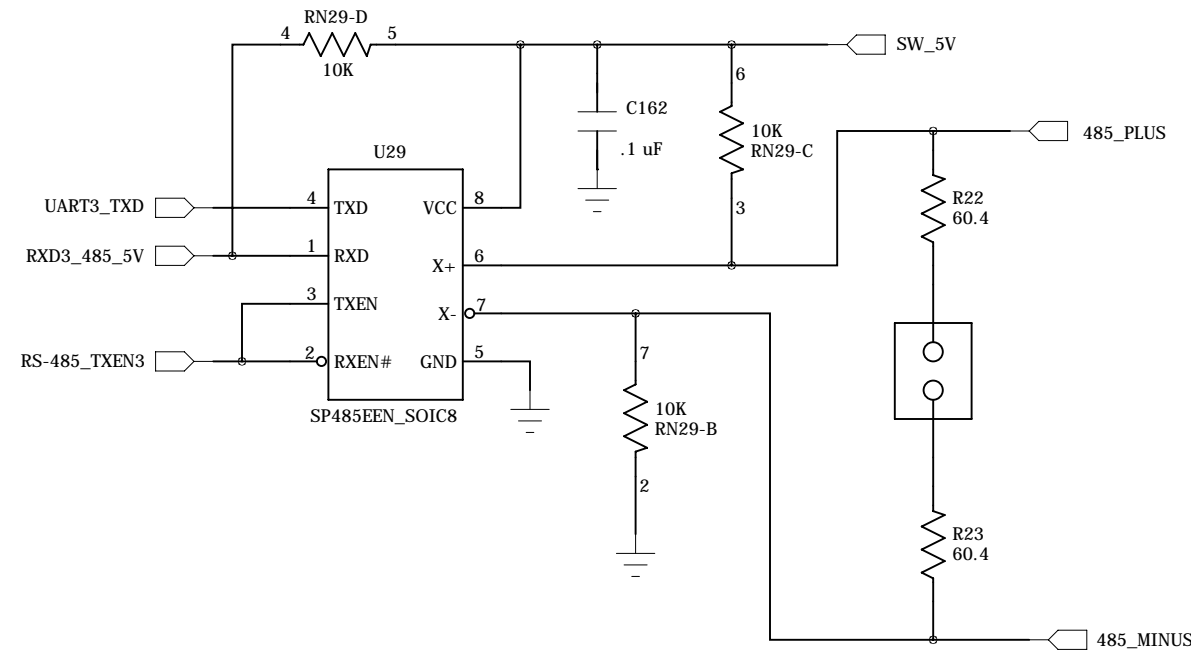
3.3V <-- 5V

Level shifter



## Dig. Input

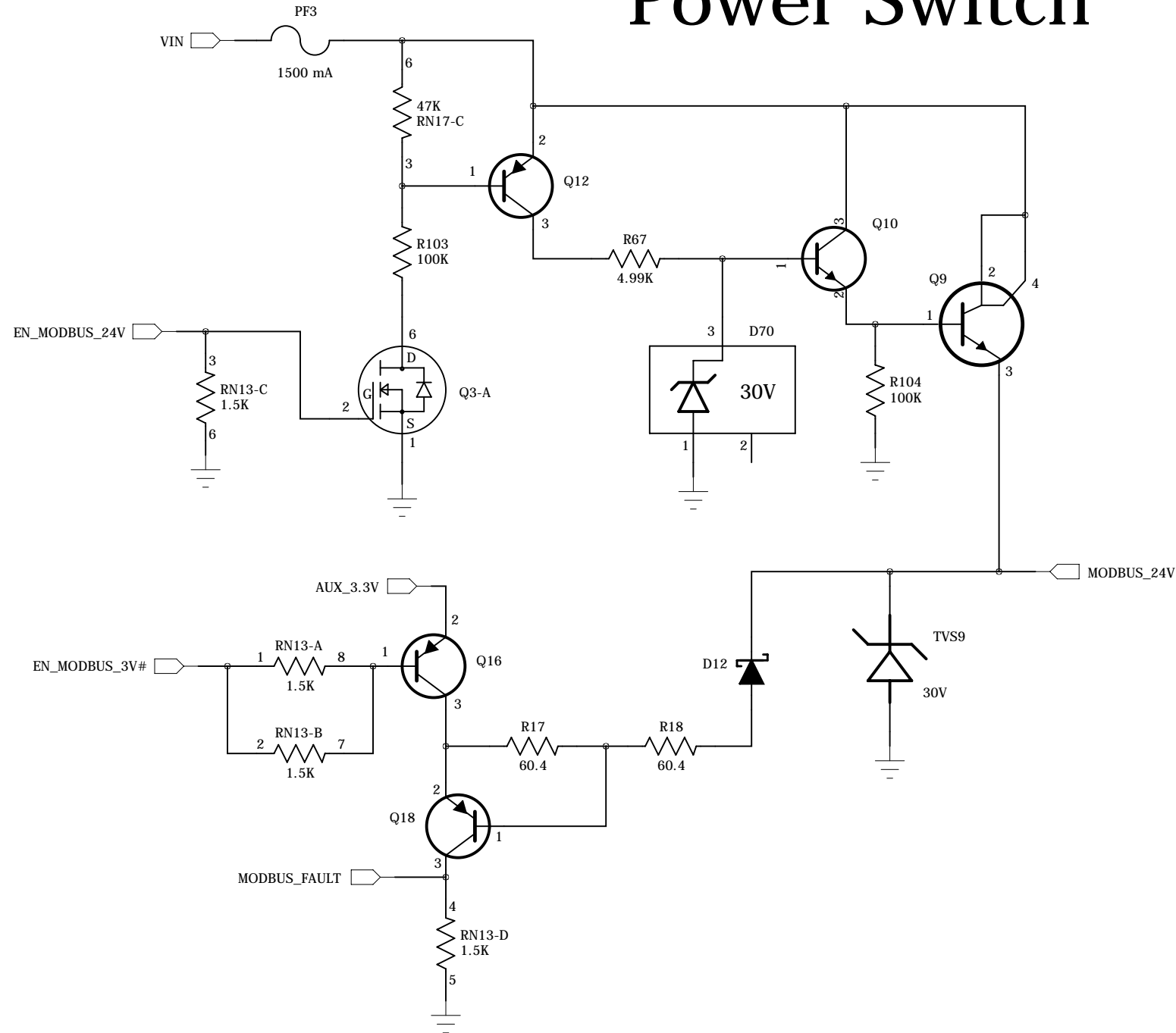
## STC RS-485 Driver



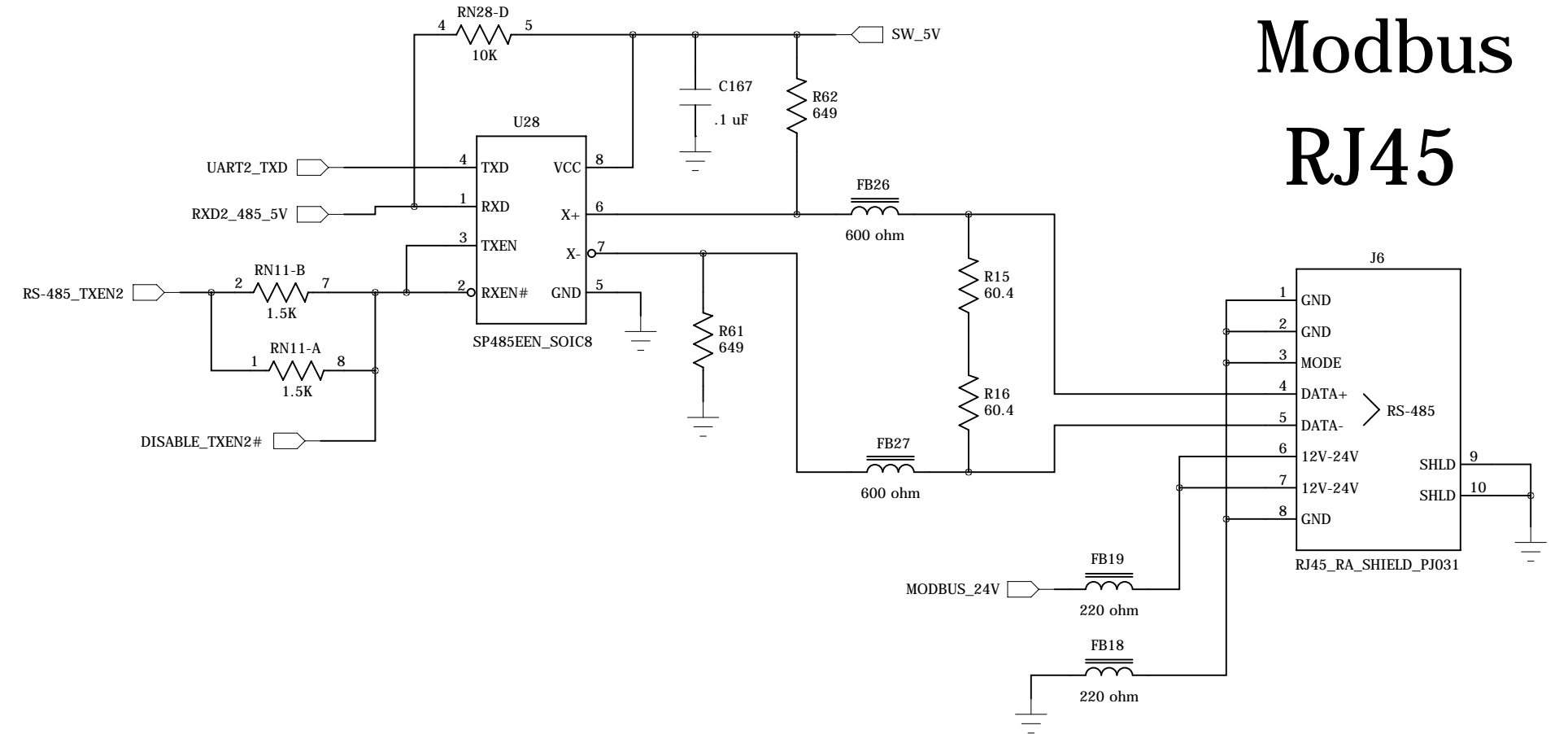
Do not use

# Mod Bus RS-485 and CAN Ports

## Modbus Power Switch

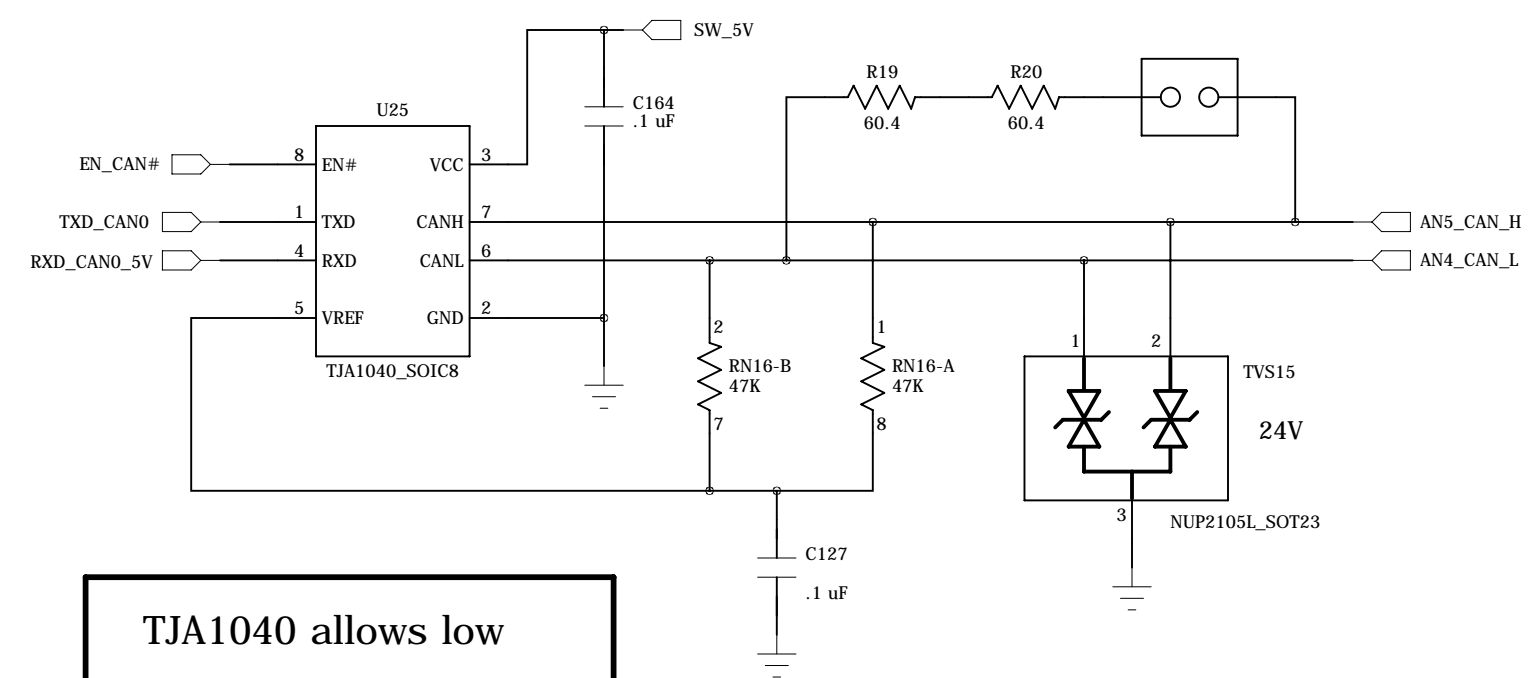


## RS-485 Driver



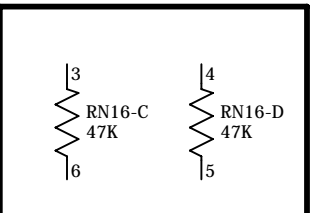
## Modbus RJ45

## CAN\_0 Transceiver

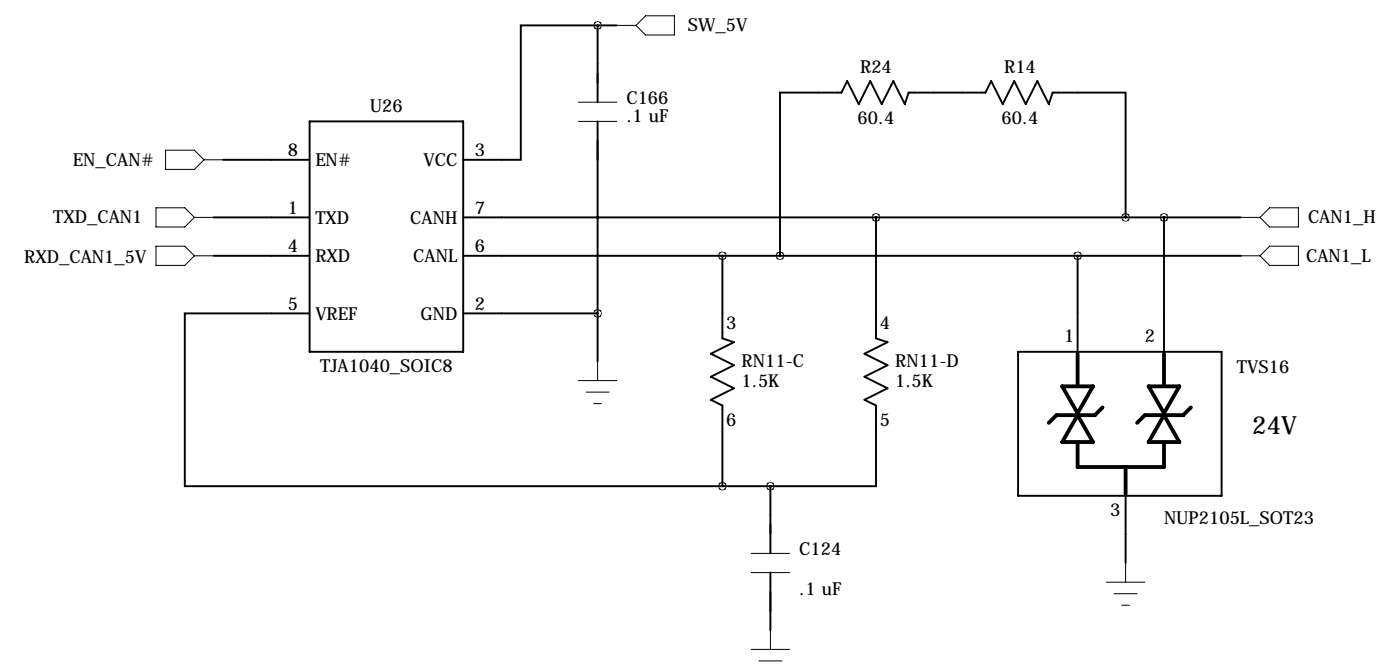


TJA1040 allows low power 15 uA mode

Do Not Use



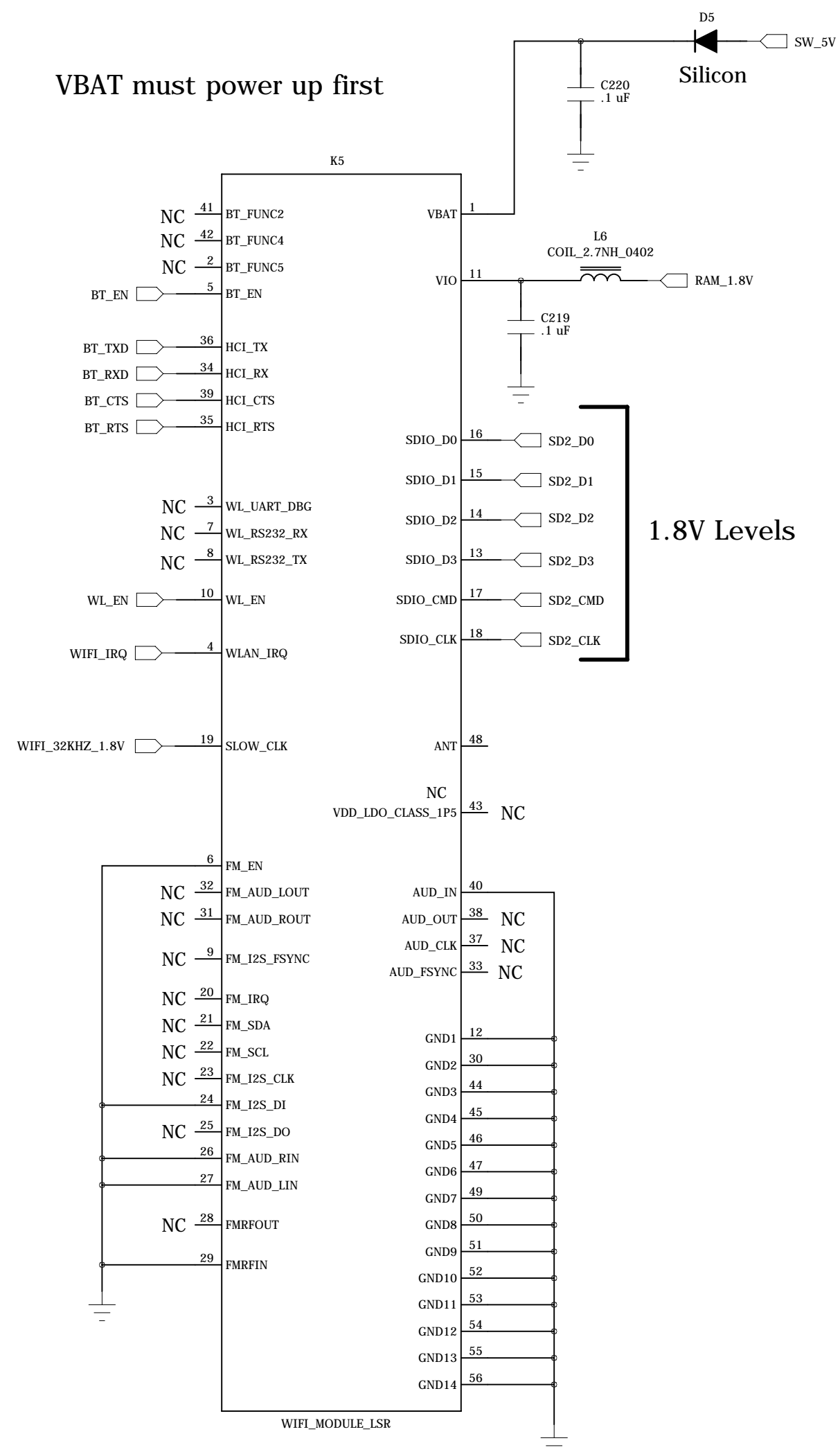
## CAN\_1 Transceiver



# WiFi Radio

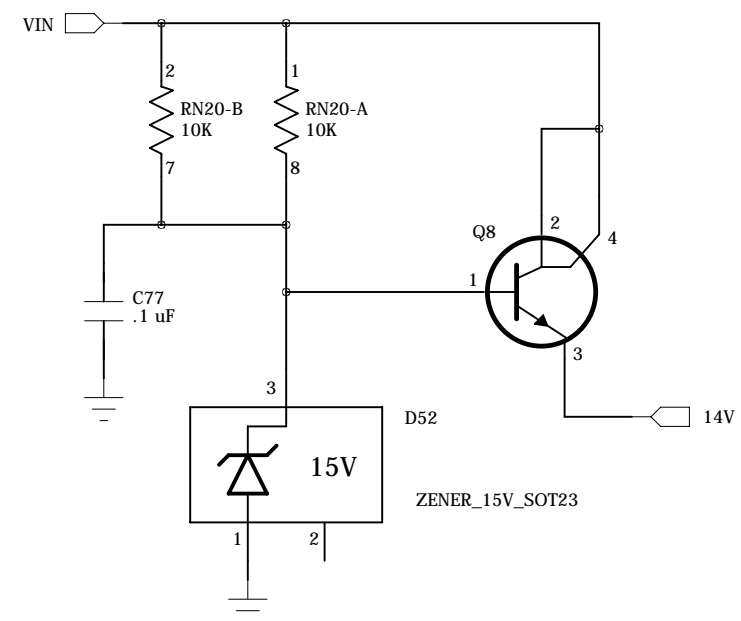
All I/O must be 1.8V levels

VBAT must power up first

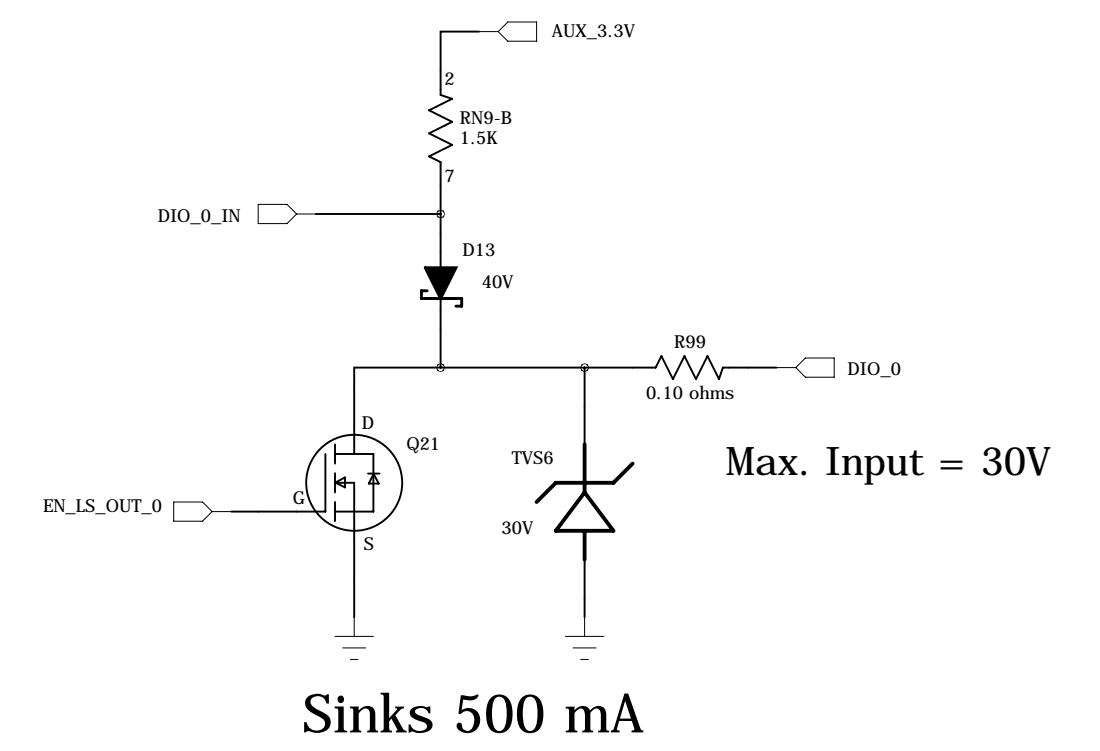


# DAC

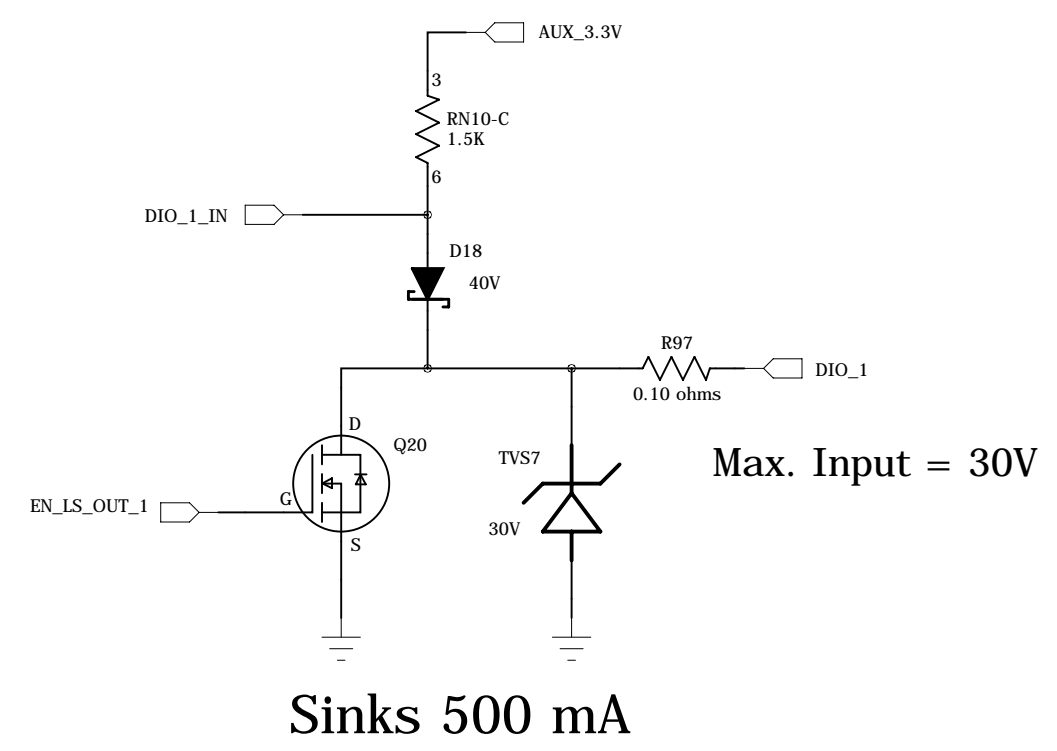
## 14V Supply



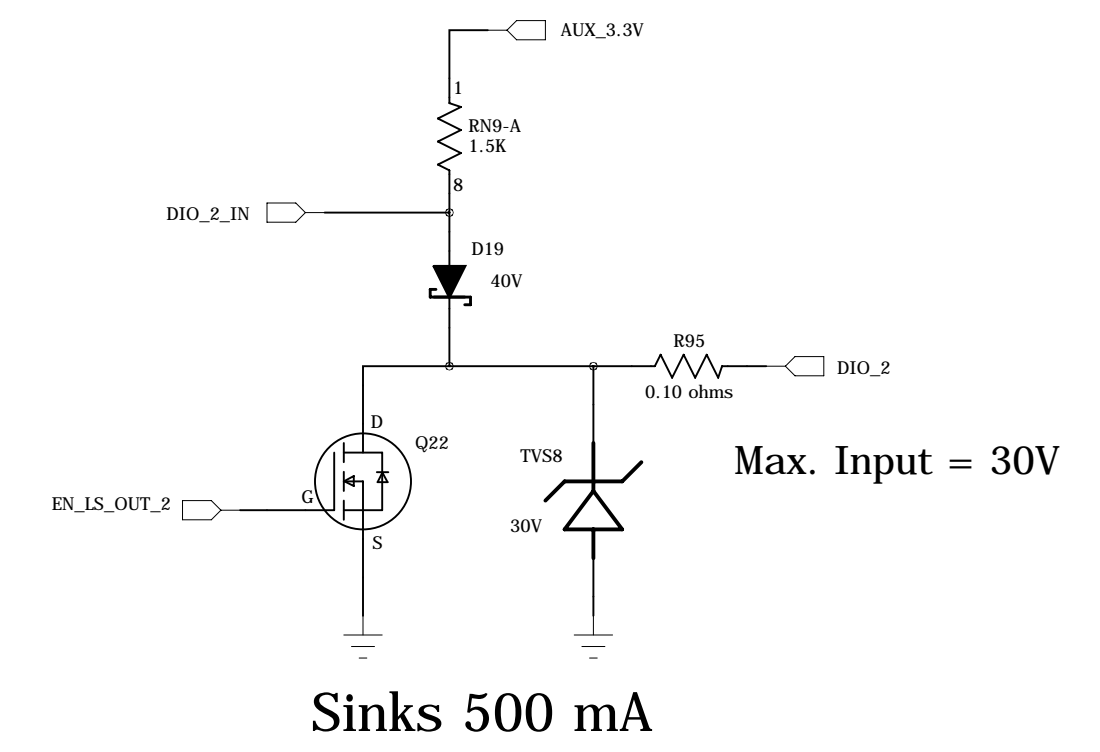
# DIO\_0



# DIO\_1



# DIO\_2



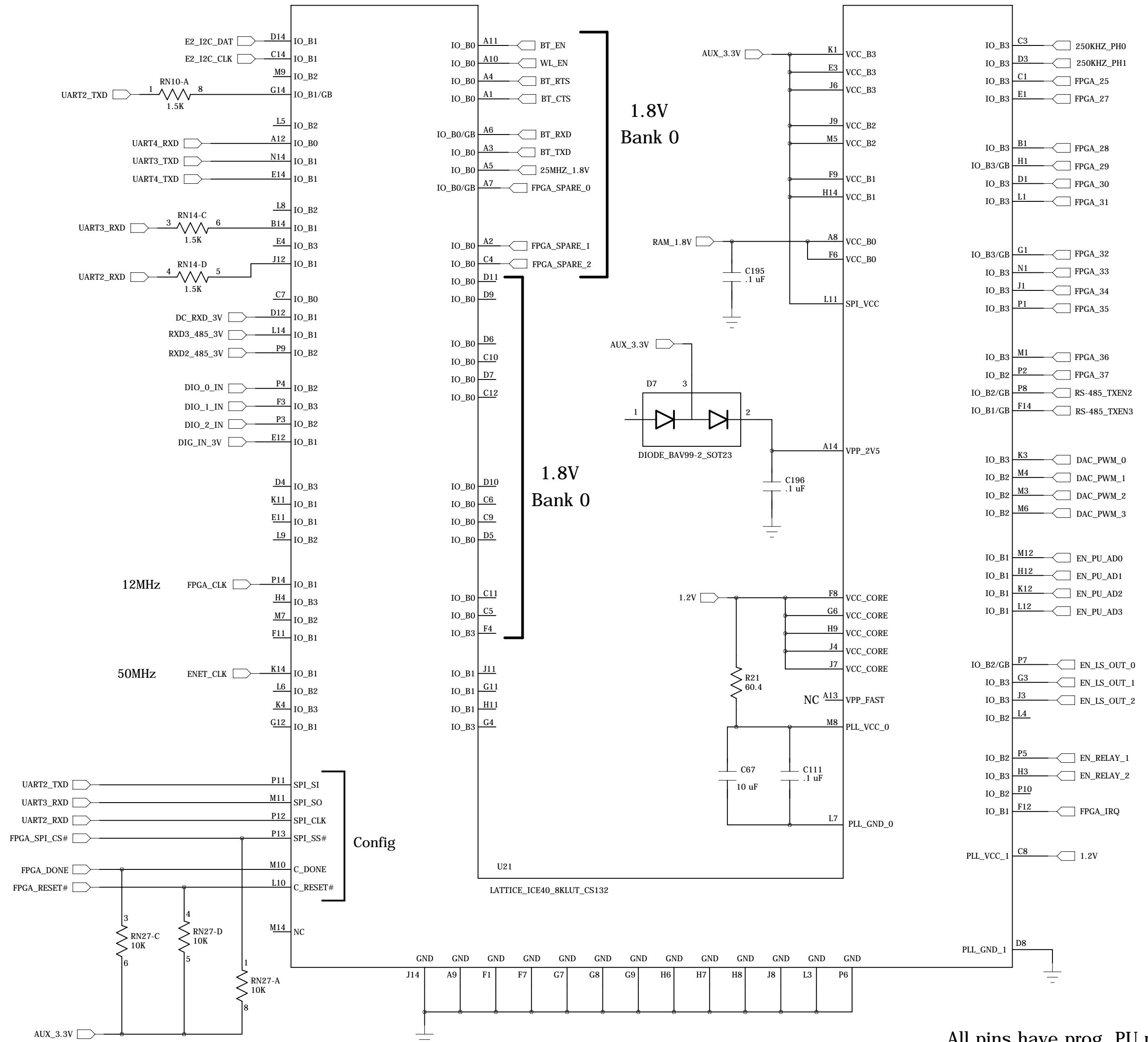
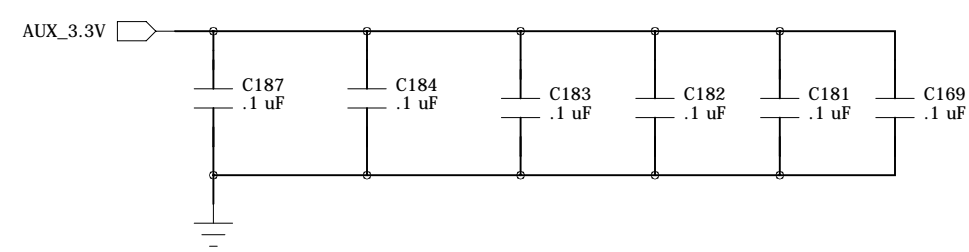
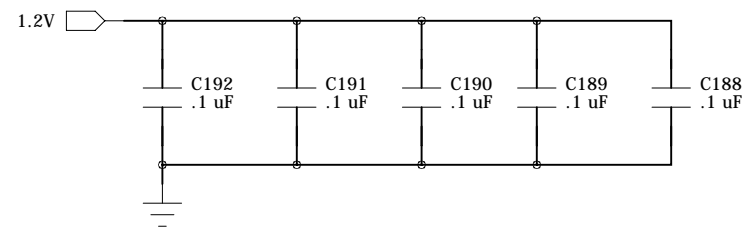
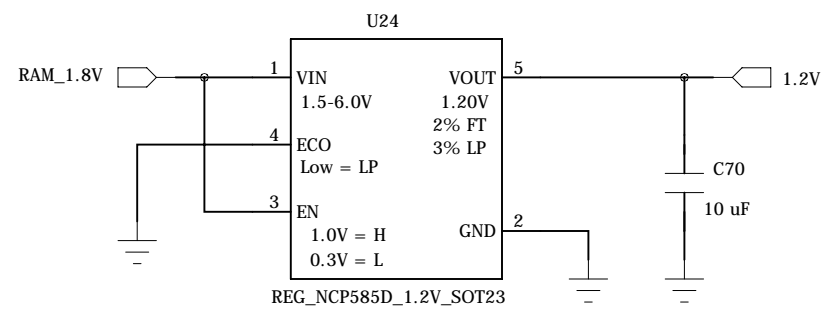
# iCE40 FPGA

## FPGA required for:

- Auto-485 for two UARTs
- PWMs for DACs
- providing serial port MUXing
- Bluetooth Level Shifting
- Additional I/O
- Daughter Card Functions

Bank 0 = 1.8V levels  
All other Banks = 3.3V

## 1.2V Regulator



PLL\_1 can not be used

If SPI\_CS# is high at POR  
FPGA configures from NVCM  
unless it is blank, then it  
tries to load from SPI Flash

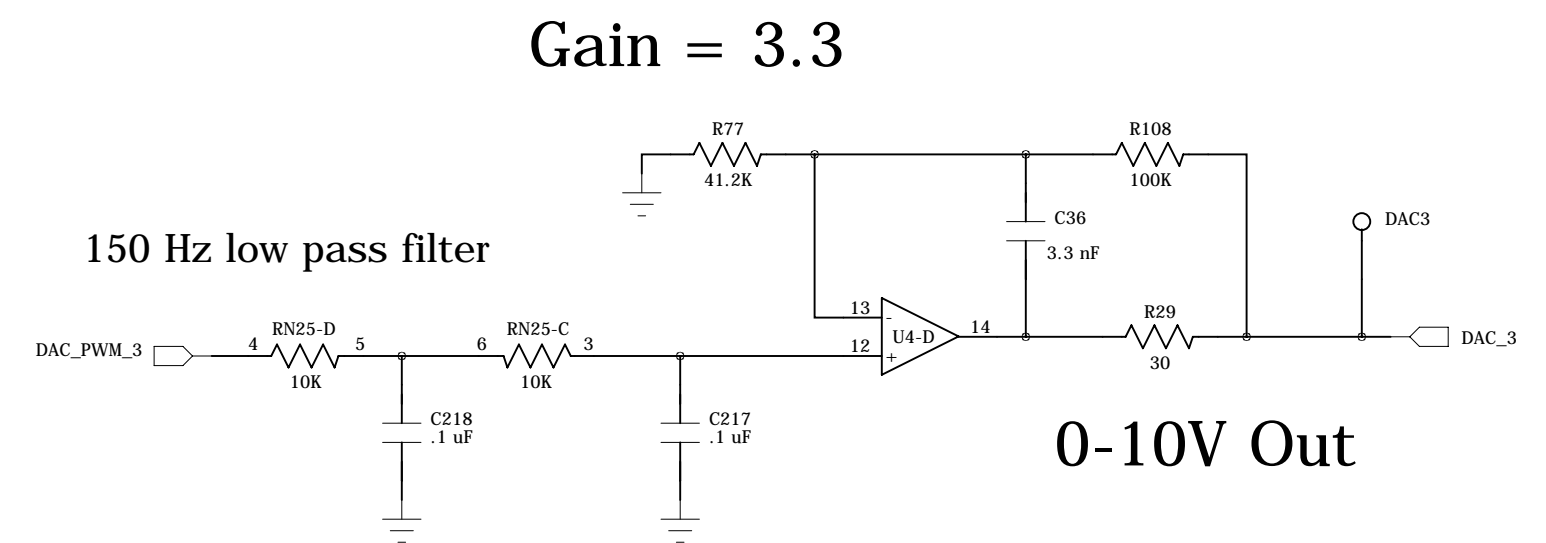
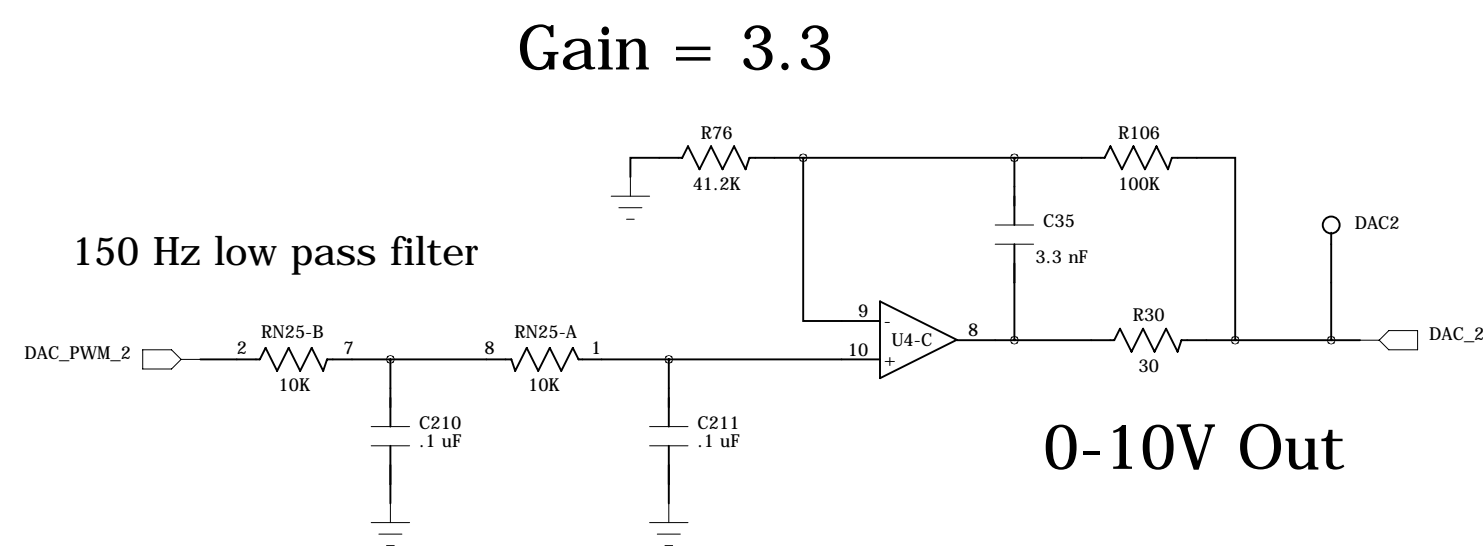
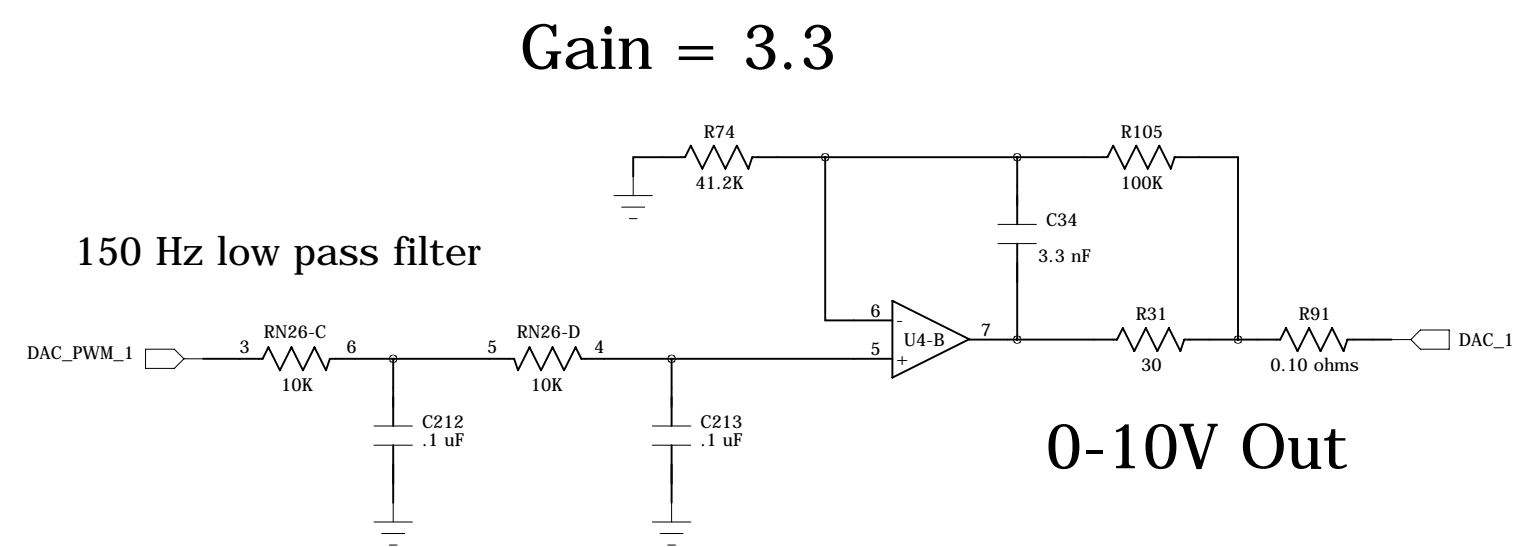
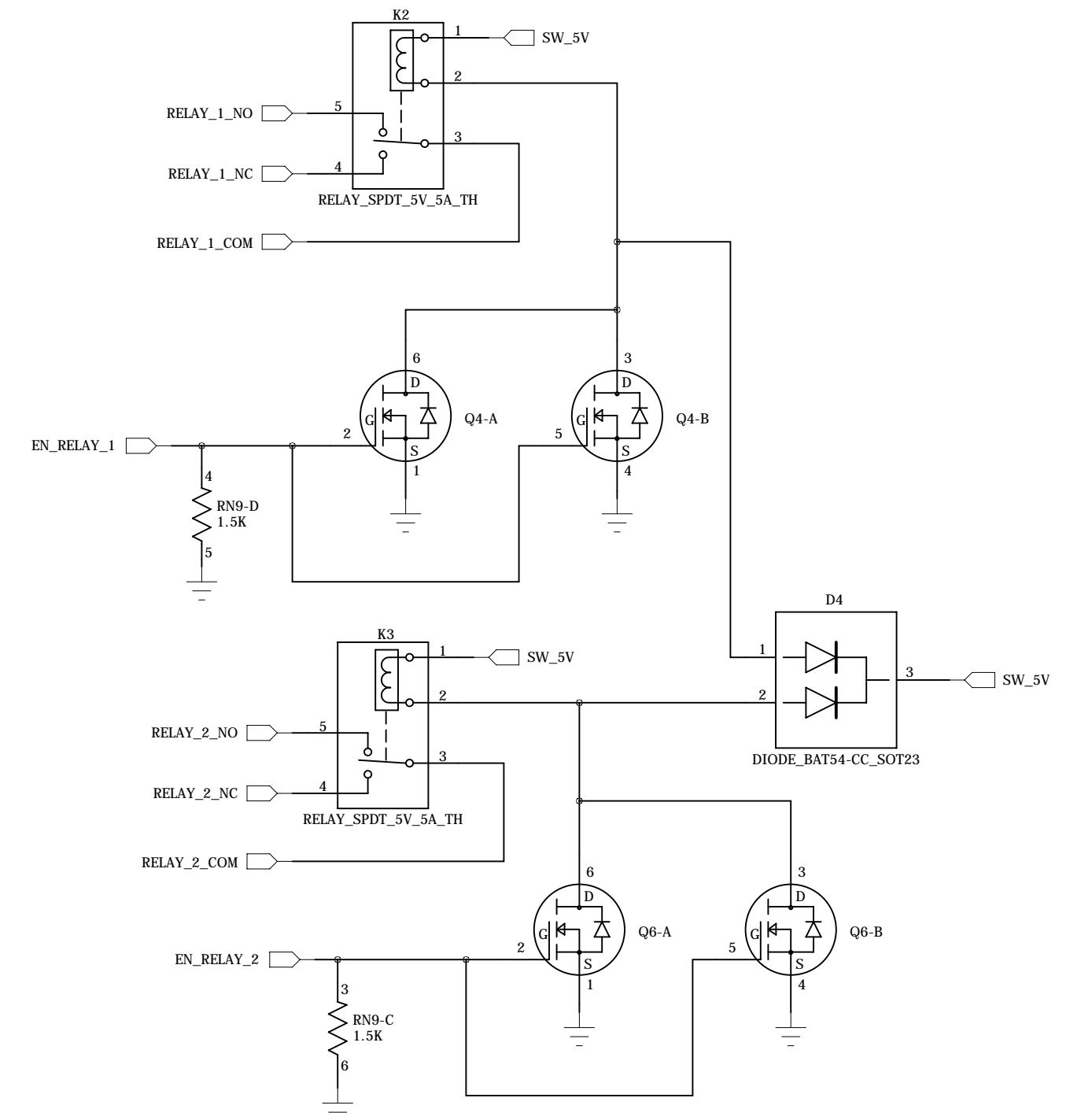
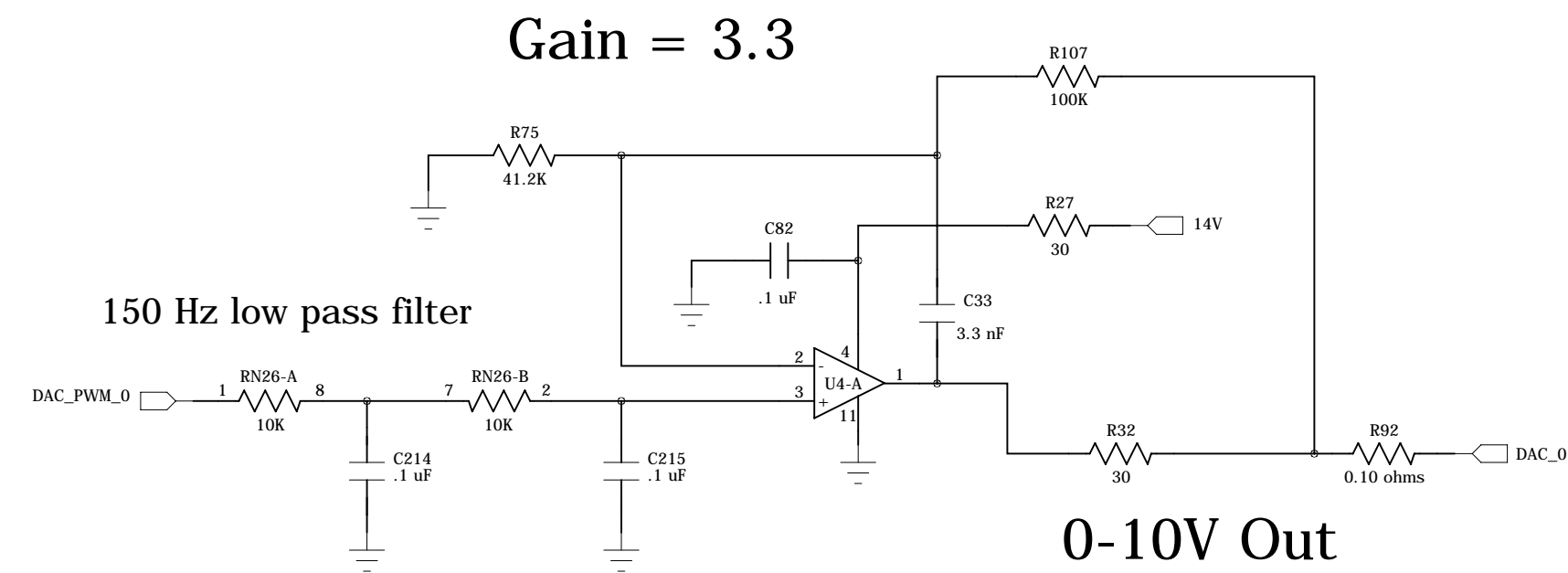
If SPI\_CS# is low at POR  
FPGA waits for external SPI  
configuration.  
Also used to write to NVCM

All pins have prog. PU resistor  
Schmitt Trig. on all Inputs  
10 MHz min clock for PLL  
No Internal clock

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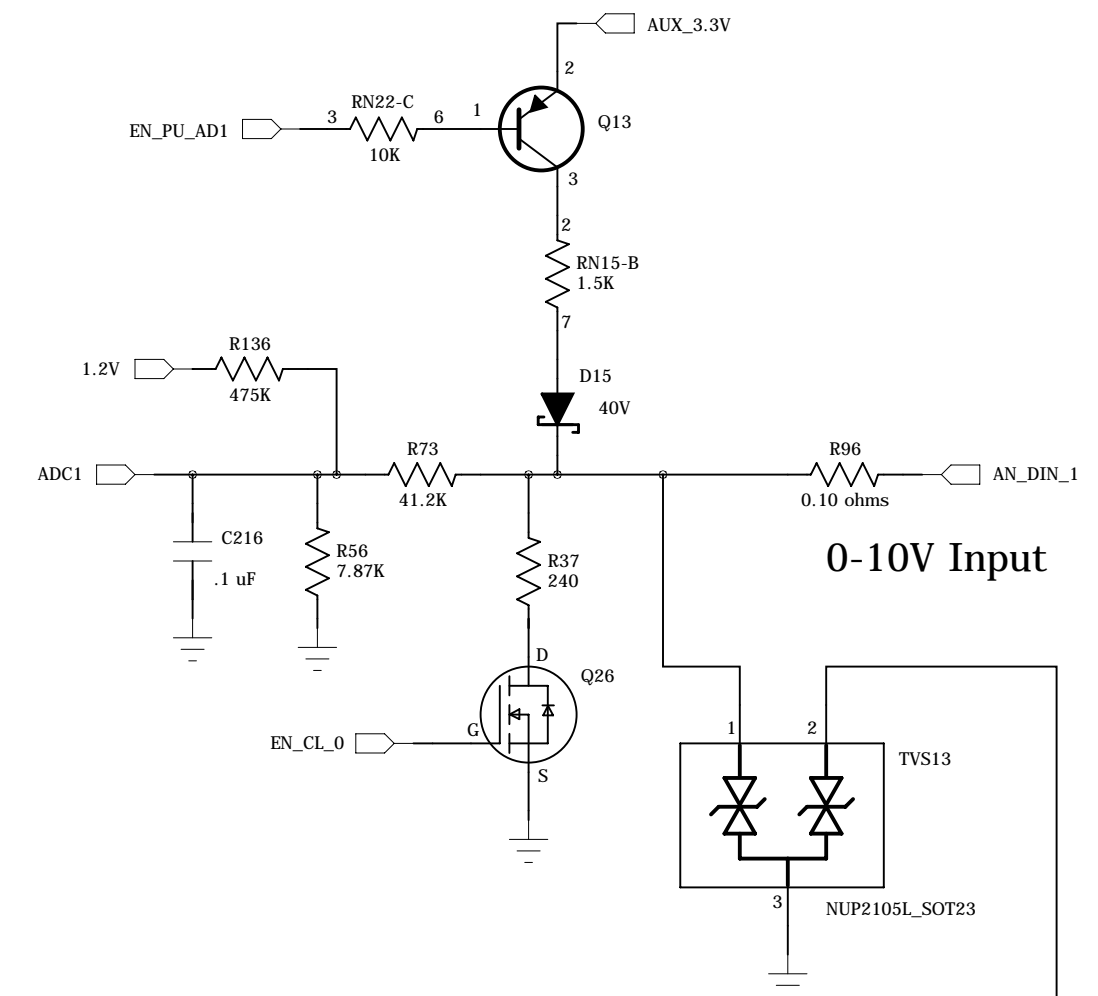
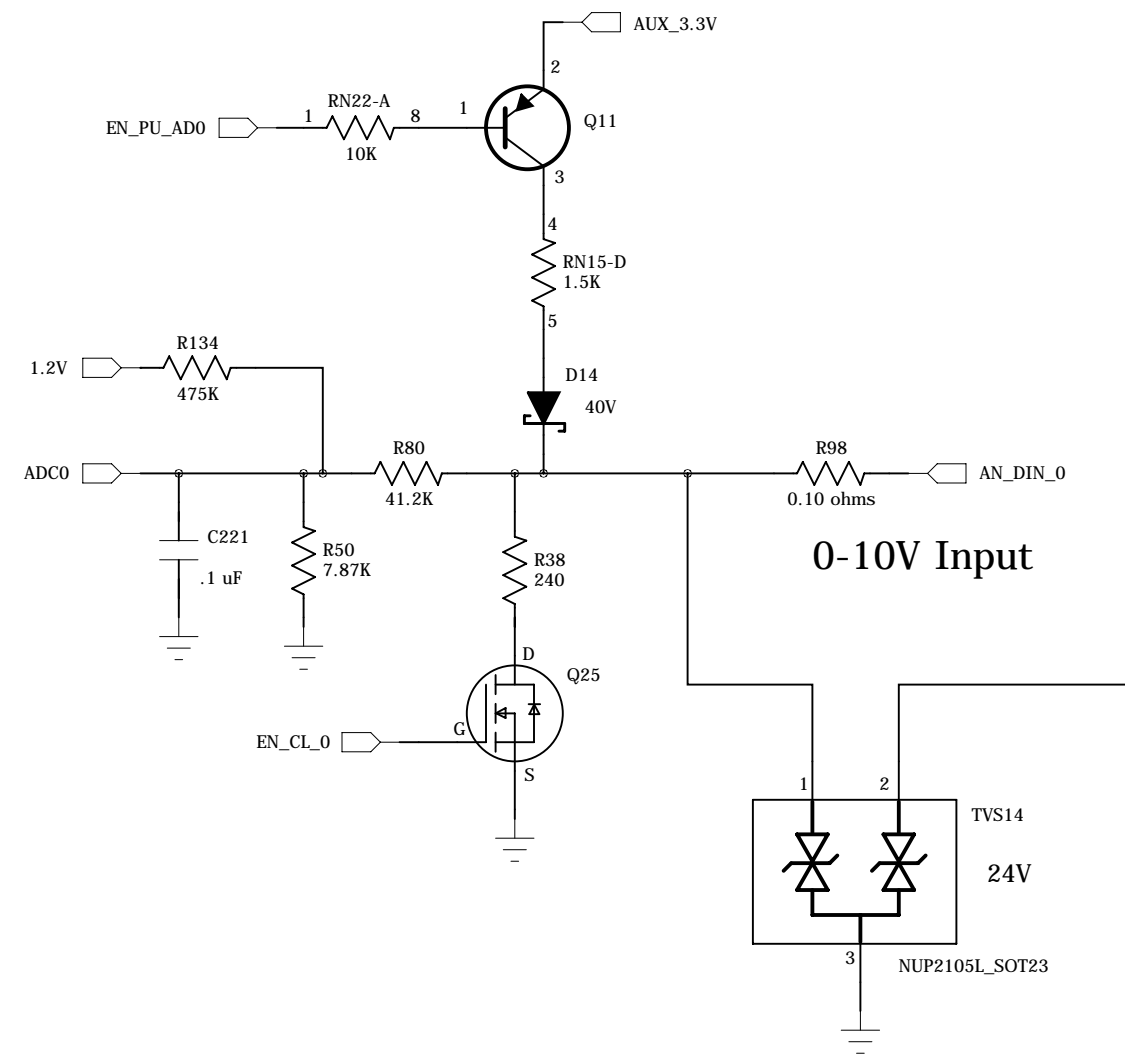
# 10-bit DACs

# Relays

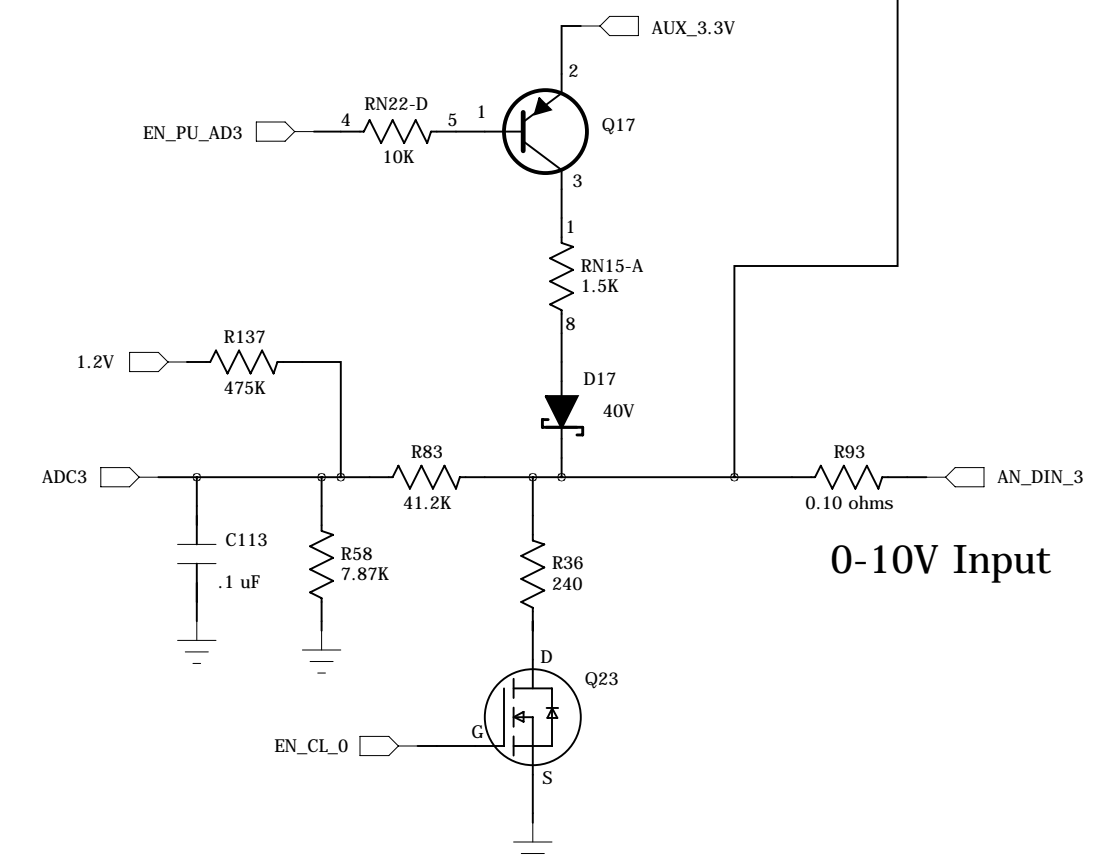
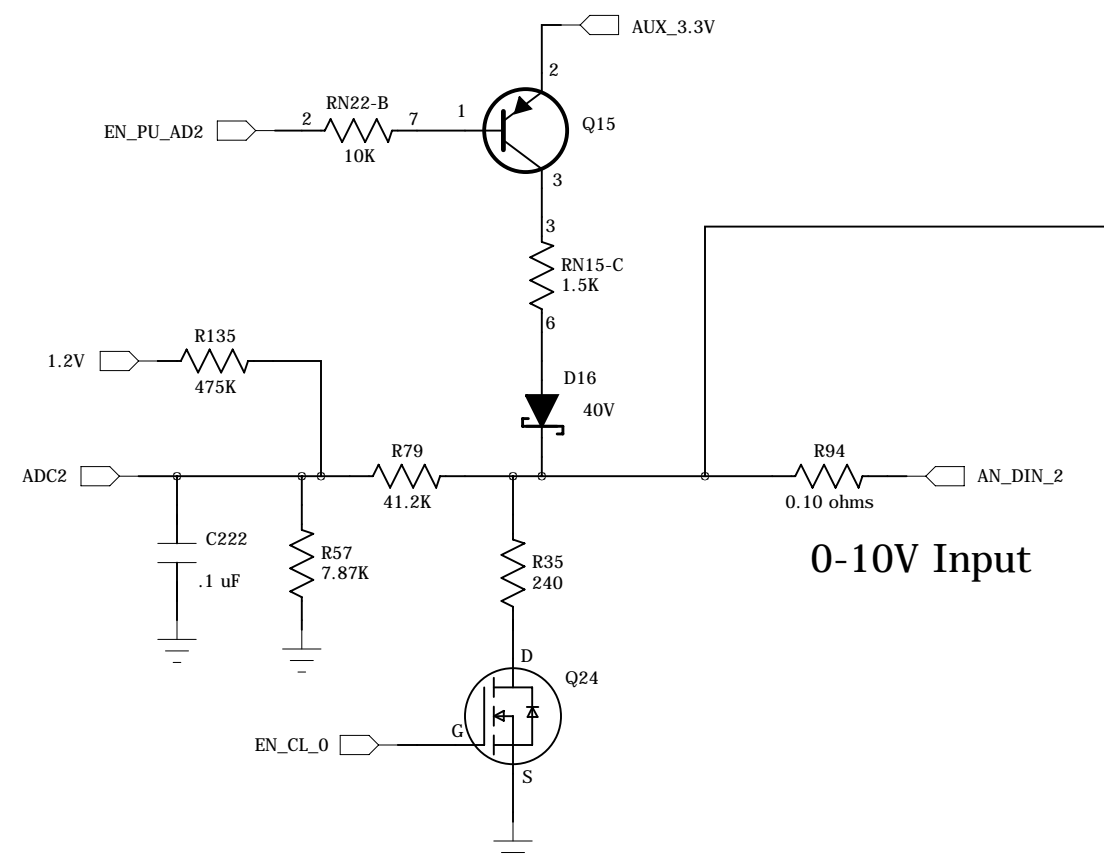




# Analog In Channels

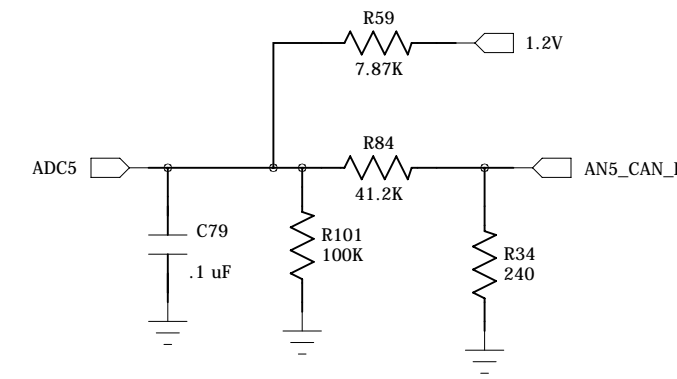
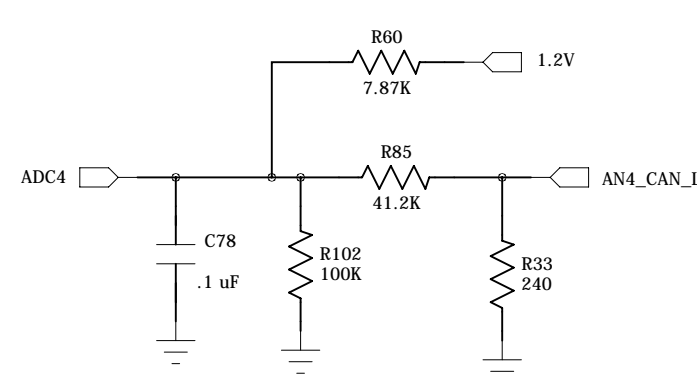


By adjusting resistor values  
All A/D Inputs can be converted  
to Bipolar, but must remove FETs



## Bipolar Analog Inputs

-5V to +5V Input Range

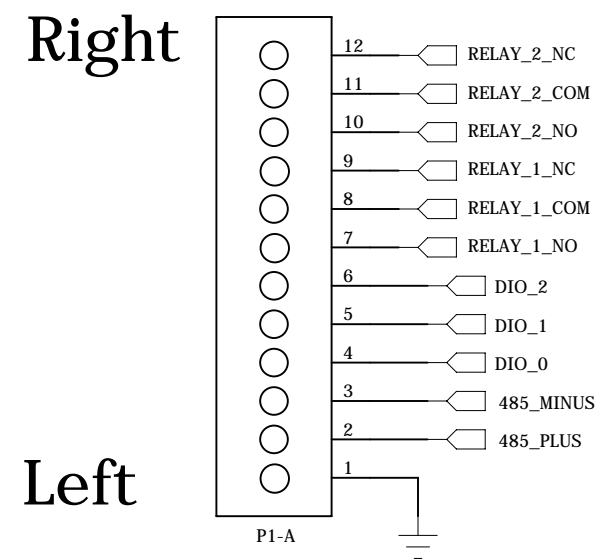


R33 and R34 not populated

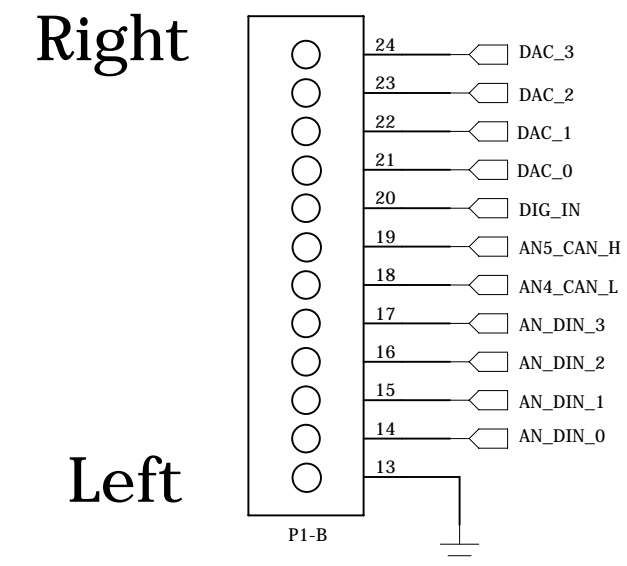
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# 24 Screw Term. Positions

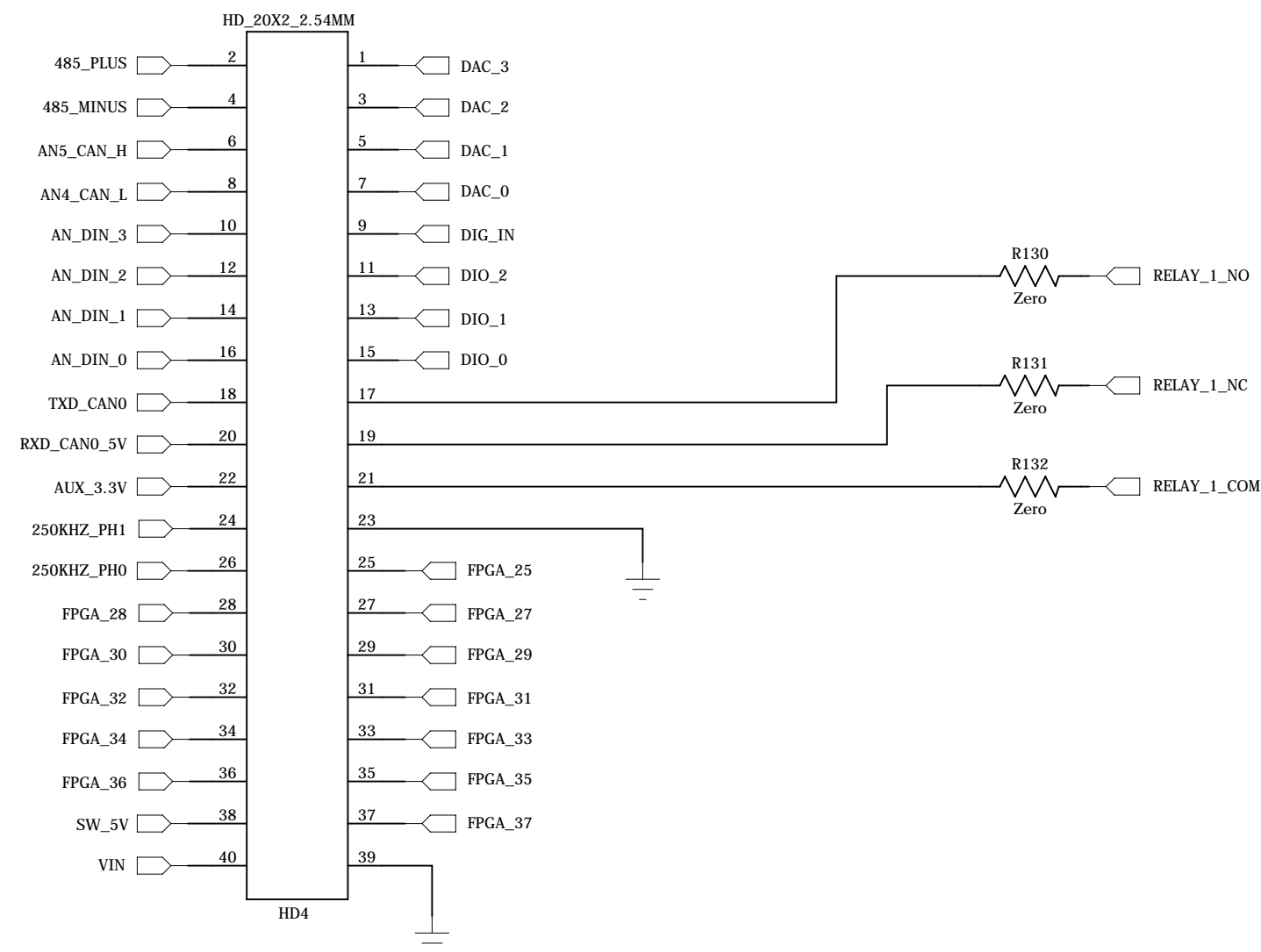
## Top Row



## Bottom Row



## DC STC Header



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