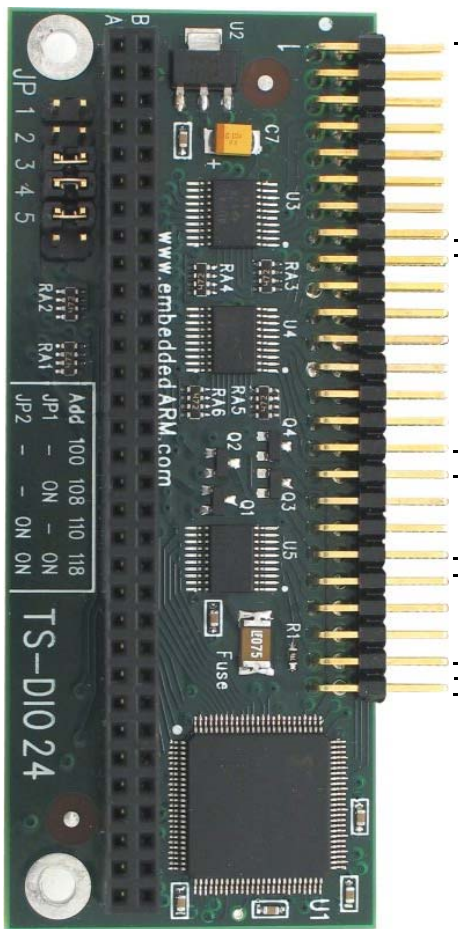


Getting started with the TS-DIO24

The TS-DIO24 is an 8-bit PC/104 expansion board that provides 24 digital I/O points. The I/O connector is an Opto-22 compatible interface that provides 16 I/O points configurable as input or output (24 mA as outputs) as well as 4 dedicated outputs capable of driving 48 mA and 4 dedicated outputs capable of sinking 1 Amp. The PC/104 interface decodes as registers in I/O space, the address is jumper selectable.

- 24 Digital I/O points
- Opto-22 compatible 50 pin connector
- 4 dedicated 48 mA outputs, 4 dedicated 1 Amp outputs
- 16 programmable I/O points
- I/O address jumper selectable
- 4 interrupt capable inputs
- Up to 4 boards in a single system.

50 pin connector pin out and electrical ratings



I/O Point Name	I/O Pin #	Ground Pin #	Signal Type
C7	1	2	<p>Port C</p> <p>Input: TTL input (4.7k Ω pullup to +5vdc) (bits0-3 interrupt capable)</p> <p>Output: 24 mA output (0-5V output drive)</p>
C6	3	4	
C5	5	6	
C4	7	8	
C3	9	10	
C2	11	12	
C1	13	14	
C0	15	16	
B7	17	18	<p>Port B</p> <p>Input: TTL input (4.7k Ω pullup to +5V)</p> <p>Output: 24 mA output (0-5V output drive)</p>
B6	19	20	
B5	21	22	
B4	23	24	
B3	25	26	
B2	27	28	
B1	29	30	
B0	31	32	
A7	33	34	<p>Port A</p> <p>Output only: 1 Amp sink (open-drain 30V tolerant)</p>
A6	35	36	
A5	37	38	
A4	39	41	
A3	41	43	<p>Port A</p> <p>Output only: 48 mA output (0-5V output drive)</p>
A2	43	45	
A1	45	47	
A0	47	48	
5V power	49	50	Auxiliary power protected by 750 mA Poly-Fuse

Transient suppression diodes required when driving inductive loads.

Register map

I/O Address	Description	Data	Bits and such
BASE + 0	Board Identifier	ASCII 'T' Read Only	ASCII 'T' equals hex 0x54
BASE + 1	reserved	Read Only	
BASE + 2	Jumper status	Read Only	Bit 0: Jumper 1 ('1'=on, '0'=off) Bit 1: Jumper 2 ('1'=on, '0'=off) Bit 2: Jumper 3 ('1'=on, '0'=off) Bit 3: Jumper 4 ('1'=on, '0'=off) Bit 4: Jumper 5 ('1'=on, '0'=off)
BASE + 3	Interrupt Control Register	(R/W)	Bit 0: PortC bit 0 connects to IRQ5 Bit 1: PortC bit 1 connects to IRQ6 Bit 2: PortC bit 2 connects to IRQ7 Bit 3: PortC bit 3 connects to IRQ9 Bit 4: IRQ5 polarity is inverted Bit 5: IRQ6 polarity is inverted Bit 6: IRQ7 polarity is inverted Bit 7: IRQ9 polarity is inverted
BASE + 4	Data Direction Register	(R/W)	Bit 0: PortC direction ('1'=output, '0'=input) Bit 1: PortB direction ('1'=output, '0'=input) Bits 2-7: reserved (The reset condition of the Data Direction Register will reflect the state of jumpers JP3-4 at power up, changes written to the DDR will override the function selected by the jumpers)
BASE + 5	Port A Data Register	(R/W)	Bits 0-7 correspond to PortA pins 0-7
BASE + 6	Port B Data Register	(R/W)	Bits 0-7 correspond to PortB pins 0-7
BASE + 7	Port C Data Register	(R/W)	Bits 0-7 correspond to PortC pins 0-7

Jumper settings for base address selection

X86 I/O address	JP2	JP1
0x100	off	off
0x108	off	on
0x110	on	off
0x118	on	on

Jumper settings for direction, ports B & C

Jumper	OFF	ON
JP3	Port C inputs	Port C outputs
JP4	Port B inputs	Port B outputs

When Port B or Port C pins are configured as outputs, the pins will reset to the low or zero state on reset.

Jumper settings for port A reset state

Jumper	OFF	ON
JP5	Outputs set to '0'	Outputs set to '1'