TS-9700 Manual

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This revision of the manual is dated

October 13, 2003

All modifications from previous versions are listed in the appendix.

Limited Warranty

Technologic Systems warrants this product to be free of defects in material and workmanship for a period of one year from date of purchase. During this warranty period Technologic Systems will repair or replace the defective unit in accordance with the following instructions:

- Contact Technologic Systems and obtain a Return Material Authorization (RMA) number and a copy of the RMA form.
- Fill out the RMA form completely and include it and dated proof of purchase with the defective unit being returned. Clearly print the RMA number on the outside of the package.

This limited warranty does not cover damages resulting from lighting or other power surges, misuse, abuse, abnormal conditions of operation, or attempts to alter or modify the function of the product.

This warranty is limited to the repair or replacement of the defective unit. In no event shall Technologic Systems be liable or responsible for any loss or damages, including but not limited to any lost profits, incidental or consequential damages, loss of business, or anticipatory profits arising from the use or inability to use this product.

Repairs made after the expiration of the warranty period are subject to a flat rate repair charge and the cost of return shipping. Please contact Technologic Systems to arrange for any repair service.

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1. Introduction

The Technologic Systems TS-9700 is a PC/104 daughter board that provides 8 channels of 12-bit Analog-to-Digital (A/D) conversion using a precision 0.2% analog reference. A single Analog Devices AD7888 chip implements the heart of the A/D subsystem. Each analog input can be individually jumper selected for one of three ranges:

0 – 2.5 Volt
0 – 10.0 Volt
0 – 20 mA

The Analog-to-Digital conversion takes 9 microseconds to complete allowing up to 100K samples per second.

The TS-9700 can optionally be populated with 4 channels of 12-bit digital-to-analog conversion using a 0.2% analog reference. Two Texas Instruments TLV5818 chips are used to implement the four Digital-to-Analog converter (DAC) outputs. Each DAC output has a rail-to-rail output buffer that allows a nominal 0 to 5 Volt output swing using a single 5V power supply.

2. PC/104 Bus Interface

The TS-9700 features an 8-bit industry standard PC/104 bus that is compatible with all Technologic Systems series of SBC. The TS-9700 requires a block of 8 bytes in the I/O space. The location of the base I/O address of this block can be selected via 3 jumpers as shown in Table 1 This allows for multiple TS-9700 boards to be used in a single system.

A Xilinx programmable logic device (PLD) is used to decode the Base I/O address. This allows for a great amount of flexibility in the standard product and allows for custom configurations if they are necessary. Call Technologic Systems for more details.

Jumper JP1	Jumper JP2	Jumper JP3	Base I/O Location
No	No	No	160 Hex
Yes	No	No	168 Hex
No	Yes	No	180 Hex
Yes	Yes	No	188 Hex
No	No	Yes	250 Hex
Yes	No	Yes	258 Hex
No	Yes	Yes	260 Hex
Yes	Yes	Yes	268 Hex

Table 1 - Base I/O Selection

3. TS-9700 Control Registers

The TS-9700 has an ID register, three registers for the A/D converter control, three registers for the DAC control, and one register that is reserved.

The TS-9700 ID register is located at I/O location Base + 1. This is a byte-wide read-only register. Reading this location always returns a fixed value of Hex 97.

Table 2 shows the I/O map for all of the TS-9700 registers.

Address	Register	Type	Notes
Base + 0	A/D Command	R/W	See Table 3
Base + 1	ID Register	Read only	Returns Hex 97
Base + 2	A/D LSB	Read only	
Base + 3	A/D MSB	Read only	Upper 4 bits = zero
Base + 4	DAC LSB	R/W	See Table 4
Base + 5	DAC MSB	R/W	
Base + 6	DAC Status	Read only	Bit 7 = Ready
Base + 7	Reserved		

Table 2

4. A/D Acquisition Cycles

The A/D command register is a byte-wide register located at I/O location Base + 0. This register can be read or written. Table 3 describes the function of each bit this register.

Bits	Notes
Bits 0-2	Selects A/D channel
Bit 3	Reserved
Bit 4	Single Acquisition Mode Single cycle = “1”
Bits 5-6	Reserved
Bit 7	A/D Acquisition Status Ready = “1”

Table 3

Any write to this register will initiate an analog-to-digital conversion with the 12-bit result being stored into the A/D LSB and A/D MSB registers. Bits 0-2 select the channel (0-7) to be converted. The result will not be available for approximately 9 microseconds (for single acquisition mode) after the command register has been written. This delay is due to the acquisition time required by the AD7888 chip. The 12-bit result can be read in a single 16-bit word cycle or as two byte reads. Since there are only 12-bits for each acquisition, the upper 4-bits of the A/D MSB register are always read as zeros. The A/D command register should be polled (read cycles only) until bit 7 is set high before attempting to read the A/D result. Bit 7 of the A/D command register is a read-only status bit that is a logic 0 while an A/D acquisition is in progress.

The TS-9700 allows two different types of acquisitions, single cycle and double cycle modes. The single cycle mode (Bit 4 = logic 1) takes 9 microseconds to complete while a double cycle requires 18 microseconds. Due to the design of the AD7888 chip, it is not possible to select the channel to convert and also convert the selected channel in a single 9 microsecond cycle. The AD7888 uses a pipelined architecture where the channel being converted is determined by the value of bits 0-2 for the previous cycle. This mode can be used for the highest sampling rate possible, but if you need to sample random channels, it is simpler to use the

double cycle mode (Bit 4 = logic 0). In the double cycle mode, the Xilinx PLD state machine does two complete acquisitions, with the first used to get the desired channel into the AD7888 chip, and the second cycle then does the acquisition on the correct channel.

5. Digital-to-Analog Converter

The DAC register is a 16-bit register located at I/O location Base + 4 and Base + 5. These registers can be read or written. These registers can be written as a single 16-bit word cycle (at Base + 4), or two byte write cycles can be used provided the lower byte is written first. Anytime the Base + 5 register is written, a DAC update cycle occurs. Table 4 describes the function of each bit this register.

Bits	Notes
Bits 0-11	Value to DAC
Bit 12	Fast DAC mode
Bit 13	Write to Buffer only
Bits 14-15	DAC Select: 0 0 = Channel # 1 0 1 = Channel # 2 1 0 = Channel # 3 1 1 = Channel # 4

Table 4

Any write to the DAC MSB register will initiate a DAC cycle with the lower 12-bits being the value written into one of the four DAC channels or into a buffer register. Bits 14,15 select the DAC channel (1-4) to be written into. Bit 13 allows the DAC value to be written into a Buffer register inside the TLV5617 chip. This buffer register acts as temporary holding register. This special cycle is implemented to allow for a simultaneous update of two DAC channels. For example, if the Bit 13 is set and Bit 15 is clear, then the DAC cycle will update the buffer in the TLV5617, but will not change any analog output. Then when a DAC cycle is run writing to Channel 2, Channel 1 will be updated with the holding register value. Both Channel 1 and Channel 2 analog outputs will change at exactly the same time. Channels 3 and 4 can also implement this simultaneous update in the same manner except Bit 15 must be set for the buffer write cycle. If simultaneous updates are not required, always leave bit 13 clear and simply select one of the four channels with bits 14 and 15.

Bit 12 set selects a fast settling time of about 3 microseconds, while Bit 12 clear will select a slower 10 microseconds. Consult the TLV5618 data sheet for details. When using the slow settling mode, the analog output has a slighter greater current sink and source capability. So this may be more desirable than the faster settling time.

6. Jumper Selection for A/D Converter

The TS-9700 uses the Analog Devices AD7888 chip to implement 8 channels of 12-bit analog-to-digital conversion. The AD7888 chip always requires a 0-2.5V input range for proper operation. The TS-9700 has 3 jumpers per A/D channel to select several different modes of operation. Please refer to Figure 1. All jumpers are labeled A, B, or C followed by the channel number. For example, for A/D channel #3, the jumpers are A3, B3, and C3.

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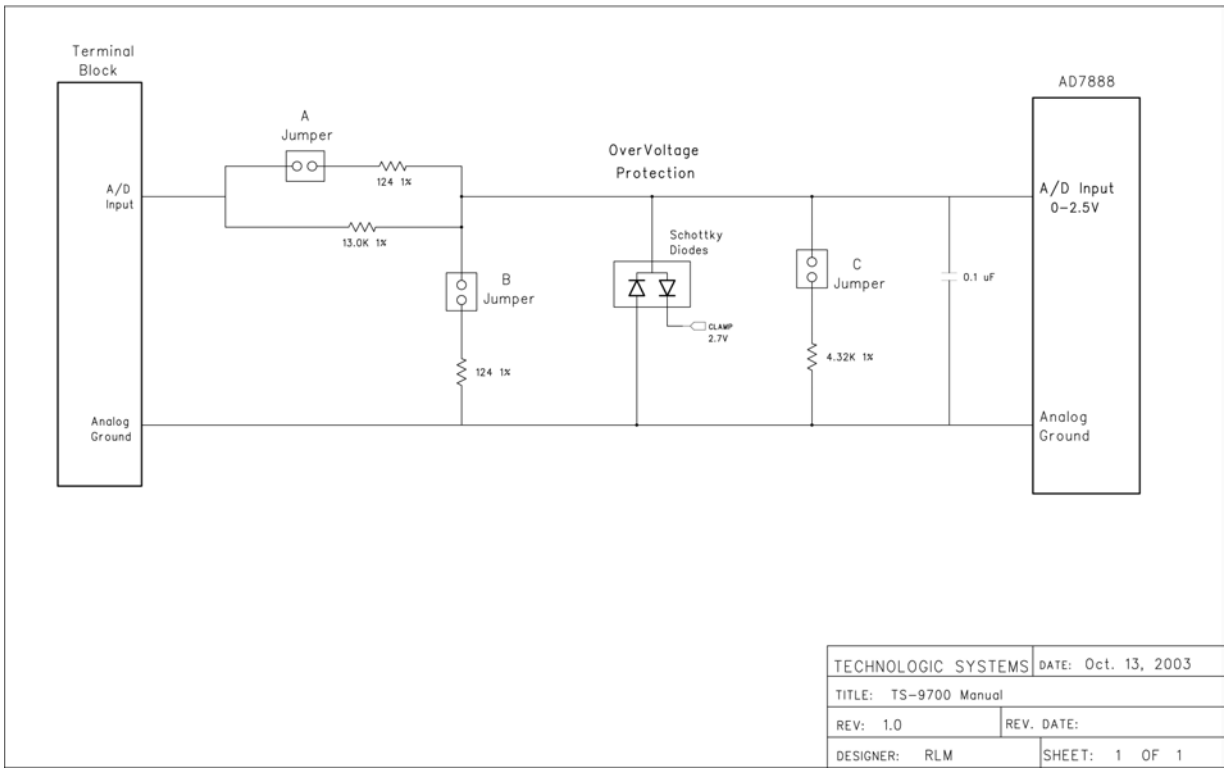

To select a 0-10V input range for a particular channel, only Jumper “C” should be installed. This causes the 4.32K and 13.0K resistors to form a 4:1 voltage divider that divides the input voltage down to 0-2.5V for the AD7888. The AD7888 does not introduce any errors due to loading, since the input impedance is several megaohms. In this mode, the bandwidth of the channel is limited to 500 Hz due to the low pass filter formed by the 0.1 uF capacitor and the nominal 3.3 Kohms source impedance in the resistive divider.

To select a 0-2.5V range, the jumpers can be positioned in two different ways. If no jumpers are installed, a low pass filter is formed by the 13.0K resistor and the 0.1 uF capacitor with a corner frequency of 120 Hz. If only Jumper “A” is installed, a 0-2.5V range is still selected, but the input resistor is lowered to 124 ohms resulting in a 10 KHz low pass filter. In both of these jumper configurations, the 0-2.5V range has the advantage of a direct conversion with no resistor dividers to introduce any errors due to resistor tolerance. The 0-2.5V range also has the advantage of an input impedance of several megaohms, compared to 17 kohm for the 0-10V range.

To select the 0-20 mA range, Jumper “A” and Jumper “B” both must be installed. A 20 mA current will produce 2.400V (20 mA x 124 ohms) into the AD7888 chip.

7. Monitoring 5V

The TS-9700 has two pads labeled JP5 near the PC/104 bus connector. If these pads are shorted, the 5V supply is connected to A/D channel # 7. This may be useful for monitoring the power supplied to the PC/104 stack. If using this feature it is required that jumper C7 be installed, and that jumpers B7 and A7 not be installed, so that A/D channel #7 is in a 0-10V range.

8. Reference Voltage

The TS-9700 uses a Texas Instruments LT1009 chip as the reference voltage for both the A/D converter and the DAC. This chip provides a 0.2% accurate 2.5V reference voltage.

If more accuracy is required, it is always possible to calibrate any channel with an external precision input to obtain more accuracy. This same technique can be used to eliminate any error introduced by resistor tolerances when using the 0-10V range or the 0-20 mA range.

9. DAC Operation

The TS-9700 uses two Texas Instruments TLV5618 chips to implement 4 channels of 12-bit digital-to-analog conversion. Each DAC output has a rail-to-rail output buffer that allows a nominal 0 to 5 Volt output swing using a single 5V power supply. The same precision 2.5V reference is used for both the A/D and DAC functions. The TLV5618 has an internal fixed gain stage of 2 that allows 0-5V output operation using the 2.5V precision reference.

This equation determines the output voltage*:* 5.000 x (code) / 4096

Where code is the 12-bit binary value (0-4095 decimal) loaded into the DAC.

The suggested load impedance on the TLV5618 should not be lower than 2 kohms. The TLV5618 can sink or source in excess of 5 mA, but when operating within .2V of either supply rail (5V and GND), the output will clipped. The TLV5618 chip is being powered by the raw 5V power to the PC/104 stack of boards. Due to limitations in the output amplifier in the TLV5618, it is helpful to run this supply voltage at the high end of its operational range. For example a 5.25V power supply voltage will allow the TLV5618 to reach its full-scale output voltage.

If running at less than 5V supply voltage, the TLV5618 chip will not lose any accuracy except near the top end of its output dynamic range. When the output is driven within 0.2V of the top supply rail, it will begin to clamp, and its linearity will not meet specifications.

10. Analog Connectors

All analog signals use plugable connectors with screw terminals. This allows for individual screw-down wires for each channel as well as a quick release for the entire group.

The A/D inputs are accessible on a 12-pin terminal block. All 8 A/D input channels are available as well as 4 analog ground connections. The pin-outs of this connector are labeled on the board silkscreen.

The A/D inputs are also accessible on a 10-pin header. This connector allows routing the analog inputs via standard ribbon cable. All 8 A/D input channels and 2 analog ground connections are available on this header. The pin-outs for this header are as follows:

Pin 1 = A/D Channel # 5
Pin 2 = A/D Channel # 6
Pin 3 = A/D Channel # 4
Pin 4 = A/D Channel # 7
Pin 5 = A/D Channel # 3
Pin 6 = A/D Channel # 8
Pin 7 = A/D Channel # 2
Pin 8 = A/D Channel # GND
Pin 9 = A/D Channel # 1
Pin 10 = A/D Channel # GND

The DAC outputs are accessible on a 6-pin terminal block. All 4 DAC channels are available as well as 2 analog ground connections. The pin-outs of this connector are labeled on the board silkscreen.

11. Drivers

Linux drivers are available for both the A/D converter and the DAC. Please Reference the Linux Developer's Manual (found through our website, www.embeddedx86.com) for further information.

Example code for DOS is available from the Single Board Computer test program. SBC-TEST.EXE is used at Technologic Systems to verify functionality of hardware prior to shipment. SBC-TEST is written in C for Borland Turbo C++ 3.0 and is available on our website: www.embeddedx86.com

Appendix A Manual Revisions

Date	Revision
10.13.03	• Document Created