Using SRAM with Technologic Systems EPCs

Technologic Systems
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Introduction

This document explains how to access the battery-backed SRAM optionally available on most Technologic Systems Embedded PCs without the use of a device driver.

Background Information

Most Technologic Systems Embedded PCs (currently the TS-2325, 2350, and 3200) have a 32 pin socket that can hold either an M-Systems DiskOnChip or a battery-backed SRAM in sizes of 32, 128, or 512KB.

Note that when using a 128 or 512KB SRAM, the EPC and battery-backed socket must be modified to accommodate the chip, making the board incompatible with the DiskOnChip and 32KB SRAM.

Details

Access to the SRAM is provided through a 32KB memory-mapped window. A read-only page latch in I/O is used to switch between the 4 (128KB) or 16 (512KB) pages of the SRAM.

IMPORTANT NOTE: The page latch is shared between both the SRAM and the resident flash disk. This simply means that you must write the desired SRAM page number to the latch before each block of SRAM accesses. Any time the A: drive is accessed (reading or writing data files or executables) the page latch will be altered, and you must re-write the latch before your next SRAM access. The BIOS flash disk driver handles the page latch for flash disk access.

To access the SRAM, write the desired page number to the latch then just read or write the desired SRAM locations.

For 128KB SRAM, the page is controlled by bits 1 and 2 (where the byte is number from a LSB of 0 to an MSB of 7) of the page latch.

For 512KB SRAM, bits 1 through 4 control the page.

In other words, shift your page number left by one bit before writing it to the latch.

PAGE LATCH ADDRESS:

072h (I/O) **bits 1 – 2 for 128KB SRAM**
bits 1 – 4 for 512KB SRAM

SRAM WINDOW:

D000:0000h – D000:8000h

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