OVERVIEW

The **TS-DIO64** is an 8-bit PC/104 (standard format) peripheral board that provides 64 digital I/O points (32 inputs plus 32 outputs) through two 34-pin locking connectors that are compatible with ribbon cables. Up to 4 TS-DIO64 boards may be installed into a single system, enabling up to 256 DIO points (128 inputs plus 128 outputs).

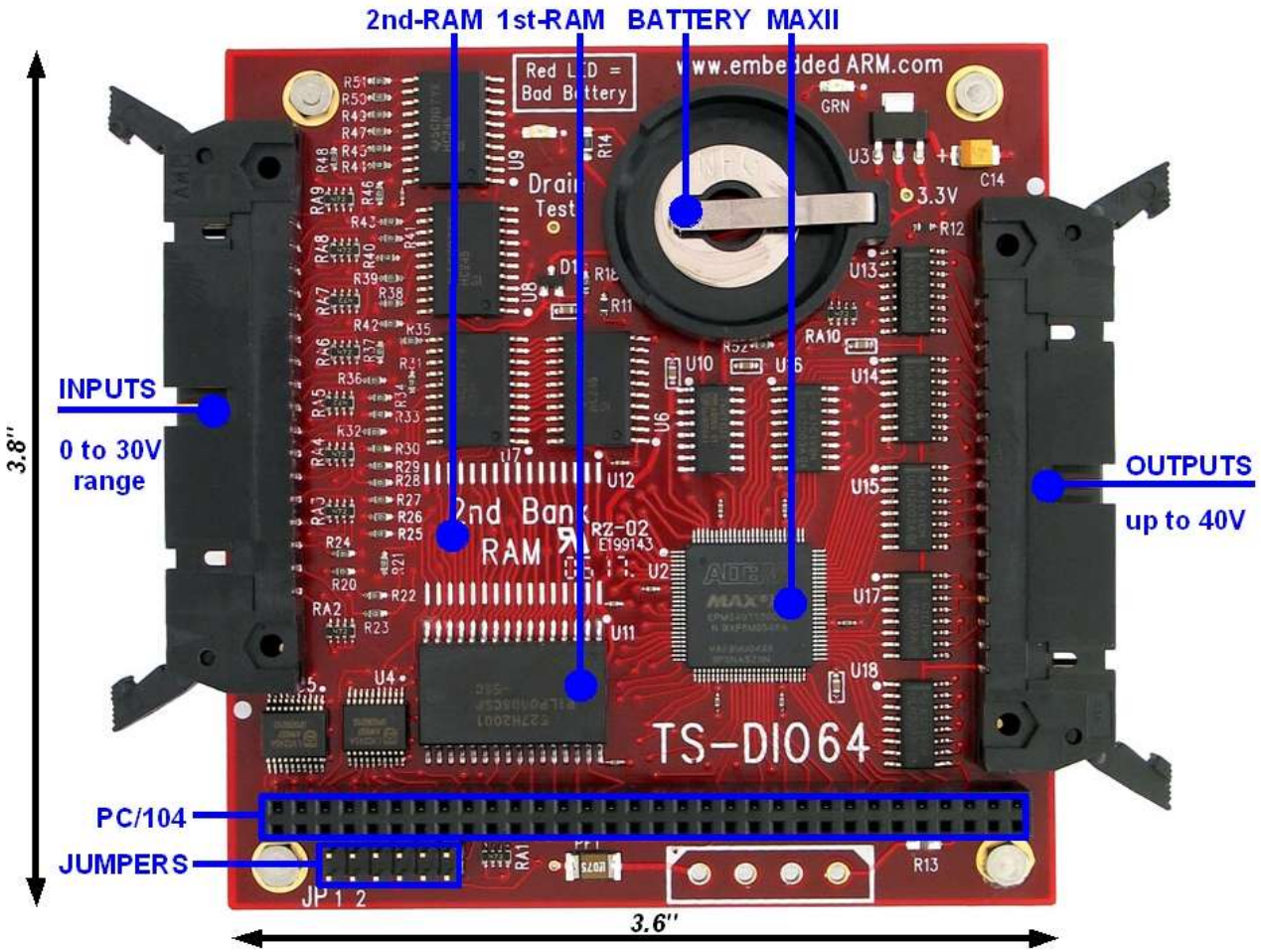
The TS-DIO64 DIO functions are compatible with any PC/104 SBC including all the Technologic Systems ARM and X86 products. **TS-DIO64** features includes:

- ✔ 32 Digital Inputs (0-30V range and 2.1V nominal threshhold)
- ✔ 32 Digital Outputs (up to 40V and 200/400 mA sink per output)
- ✔ 4 regions of I/O address jumper selectable
- ✔ **RoHS** compliant (Restriction of Certain Hazardous Substances)
- ✔ Optional 512 KByte or 1 MB battery-backed SRAM
- ✔ Optional 34 Pin 18" Ribbon Cables with locking connectors

The optional battery-backed SRAM is decoded in ISA memory space at a location determined by the SRAM control register (see Register Map).

> **Note**
> The Battery-backed SRAM option is only designed to work with the TS-7000 series SBC's (TS-ARM products only).

PRODUCT VIEW



TS-DIO64 shown with optional 512K battery-backed SRAM

HARDWARE CONFIGURATION

I/O ADDRESS

The PC/104 interface decodes as registers in a 16-byte wide I/O space; the base address is jumper selectable.

Jumper settings for I/O address space selection

I/O Address	JP1	JP2
0x100	OFF	OFF
0x110	ON	OFF
0x120	OFF	ON
0x130	ON	ON

Note
TS-ARM (TS-7000 SBC's) I/O space starts at **0x11E0_0000** physical address. e.g. 0x100 I/O space is decoded at 0x11E0_0100 physical memory

LEDs

The on-board **red** LED indicates the Lithium battery health. Typical lifetime of the battery is over 10 years. When the red LED is ON, the battery needs replacement, but this does not mean that the battery-backed RAM contents are corrupted. The battery can be purchased from Digikey, part number #P340-ND (Panasonic manufacturer part number is #CR2450).

The on-board **green** LED is an SRAM activity indicator. It pulses during read/write activity on the PC/104 bus.

INPUT CONNECTOR

On the 34-pin **input** connector, pins 1 to 32 are used for 32 total digital inputs. Pin 33 is fused 5V and the current is limited with a PolyFuse to 750 mA. Pin 34 is ground. Any voltage above 3.0 volts on the input pins will return a logic "1", while any voltage below 1.2 volts will return a logic "0". Each input can be driven from 0 to +30V, and all inputs have a 4.7K ohm resistor pull-up to 5V

OUTPUT CONNECTOR

On the 34-pin **output** connector, pins 1 to 32 are used for 32 total digital outputs. Pin 33 is clamp voltage and pin 34 is ground. 22 outputs (pins 1 to 22) can sink 200 mA, while 10 outputs (pins 23 to 32) can sink 400 mA. These can be mounted in parallel to get much higher current drive. All outputs pins can sink up to 40V loads.

Writing a logic "1" to the output register bits will turn on the sink darlington transistor, forcing the output to below 1.2V. Writing a logic "0" will turn off the sink darlington transistor, and the output will be floating (not forced high). All output registers are initialized to zero at power up or system reset, which means that all outputs are turned off by default (not sinking current).

Note
The clamp pin should be connected to the highest voltage being used for loads. For example, if the outputs are driving 24V solenoids and 12V relays, then pin 33 should be connected to the 24V power supply. This will protect the output transistors from reverse EMF "transients" that may exceed 40V if the clamp pin was not connected to 24V.

BASE REGISTER MAP

The **TS-DIO64** uses 16 registers of 8-bits each (16 bytes total) which appear at the jumpered I/O base address. All input and output DIO registers are initialized at power up or system reset to zero by default.

I/O Addr	Description	Data Access	Bits and such
Base+0x0	Board identifier	Read only	reads 0xA4 unique ID to verify presence
Base+0x1	PLD revision and options	Read only	reads PLD rev and options bit 7:5 = reserved bit 4 = SRAM option present (1=on, 0=off) bit 3:0 = PLD revision (1=revA)
Base+0x2	SRAM control register	R/W *bits 1 and 0 are read only	bit 7:5 = reserved bit 4 = makes SRAM appear in memory space (1=enable, 0=disable) bit 3:2 = SRAM memory space address decode 0=0x0 (0x1180_0000 ARM) 1=0x10_0000 (0x1190_0000 for TS-ARM) 2=0x20_0000 (0x11a0_0000 for TS-ARM) 3=0x30_0000 (0x11b0_0000 for TS-ARM) bit 1 = battery status (1=ok, 0=bad) (R/O) bit 0 = external power status (1=on, 0=off) (R/O)
Base+0x3	reserved		
Base+0x4	DIO output #1	R/W	Pins 1 to 8 - pin 1 is bit 0 (logic “1” = enables current sink to ground)
Base+0x5	DIO output #2	R/W	Pins 9 to 16 - pin 9 is bit 0 (logic “1” = enables current sink to ground)
Base+0x6	DIO output #3	R/W	Pins 17 to 24 - pin 17 is bit 0 (logic “1” = enables current sink to ground)
Base+0x7	DIO output #4	R/W	Pins 25 to 32 - pin 25 is bit 0 (logic “1” = enables current sink to ground)
Base+0x8	DIO input #1	Read only	Pins 1 to 8 - pin 1 is bit 0 (logic “1” if input > 3.0V, logic “0” if input < 1.2V)
Base+0x9	DIO input #2	Read only	Pins 9 to 16 - pin 9 is bit 0 (logic “1” if input > 3.0V, logic “0” if input < 1.2V)
Base+0xA	DIO input #3	Read only	Pins 17 to 24 - pin 17 is bit 0 (logic “1” if input > 3.0V, logic “0” if input < 1.2V)
Base+0xB	DIO input #4	Read only	Pins 25 to 32 - pin 25 is bit 0 (logic “1” if input > 3.0V, logic “0” if input < 1.2V)
Base+ 0xC-0xF	reserved		

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