OVERVIEW

The **TS-POE100** is a PC/104 peripheral board (standard format) that provides a 10/100 Ethernet port integrated with a Power-over-Ethernet splitter circuit, which is capable to provide up to 12W of power through the PC/104 bus.

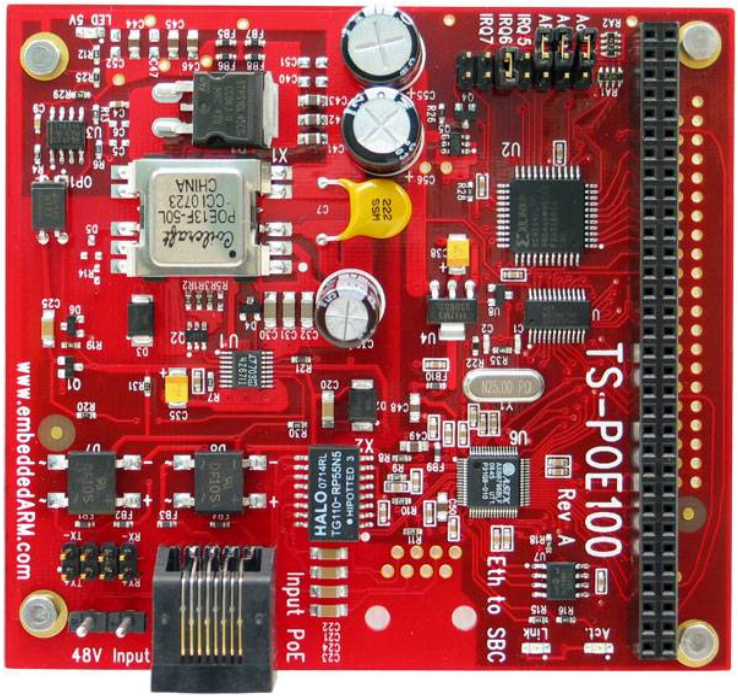
The TS-POE100 is compatible with both Technologic Systems x86 and ARM single board computers. **TS-POE100** features include:

- ✔ Power-over-Ethernet Splitter
- ✔ Integrated 10/100 Ethernet Port
- ✔ 2.4 amp @ 5V (12W)
- ✔ Provides regulated 5VDC to SBCs through PC/104 connector
- ✔ Jumper selectable I/O and IRQ
- ✔ Isolated power
- ✔ PC/104 Dimensions 3.6 x 3.8 inches
- ✔ Wake-on-LAN integrated with PoE
- ✔ Programmable sleep modes
- ✔ Linux driver and utilities available
- ✔ **RoHS** compliant (Restriction of Certain Hazardous Substances)

The **TS-POE100** features a Linear Technology LTC4267 PoE chip fully compatible with the IEEE 802.3af specification. The TS-POE100 is a Power-over-Ethernet splitter interface that provides up to 12W (2.4A @ 5V) to external devices (class 3 devices). The internal switching-regulator delivers regulated 5VDC to the PC/104 connector, enabling a complete stackable SBC system to be powered.

In addition, the **TS-POE100** provides an integrated 10/100 ethernet port through the ASIX AX88796B embedded MAC with on-chip PHY. It interfaces with the PC/104 connector via 16-bit data bus and the register map is NE2000 compatible. The ASIX solution features Wake-on-LAN functionality, enabling the Ethernet chip to enter in sleep mode with programmed wake-up on the recepetion of a magic network package. Once integrated with the PoE, this function allows a complete SBC system to enter power-save mode and to wake-up through the network whenever required.

PRODUCT VIEW



HARDWARE CONFIGURATION

The **TS-POE100** jumpers select one-of-three IRQ lines and one-of-four I/O address regions. Also, it is possible to do PC/104 16-bit access using only the 64-pin PC/104 connector in ARM mode if the ARM jumper is ON. Jumpers IRQ5, IRQ6 and IRQ7 (ARM IRQs 22, 33 and 40, respectively) selects the desired ISA IRQ line for the TS-POE100 MAC.

I/O ADDRESS

The PLD and MAC I/O address locations can be configured using jumpers Add1 and Add2 according to the table below:

Jumper settings for I/O address space selection

PLD I/O	MAC I/O	Add1	Add2
0x100	0x200	OFF	OFF
0x110	0x240	ON	OFF
0x120	0x300	OFF	ON
0x130	0x340	ON	ON

Note
TS-ARM (TS-7000 SBC's) I/O space starts at **0x11E0_0000** physical address. e.g. 0x100 I/O space is decoded at 0x11E0_0100 physical memory

BASE REGISTER MAP

The **TS-POE100** has 4 registers of 4-bits each which are implemented on the PLD.

I/O Addr	Description	Data Access	Bits and such
Base+0x0	Board identifier	Read only	returns 0x5 unique ID to verify presence
Base+0x4	PLD revision	Read only	Returns PLD revision
Base+0x8	SRAM control register	Read only	bit 3 = IRQ7 jumper status (1=ON, 0=OFF) bit 2 = IRQ6 jumper status (1=ON, 0=OFF) bit 1 = IRQ5 jumper status (1=ON, 0=OFF) bit 0 = ARM jumper status (1=ON, 0=OFF)
Base+0xC	Power control	Bit 0 is RW	bit 3:1 = reserved bit 0 = 5VDC power to PC/104 bus control (1=power ON, 0=power OFF)

For a complete description of the MAC register map (which is NE2000 compatible), please refer to the ASIX AX88796B documentation.

POWER INPUT AND ASSEMBLY

In order to power up a system including a PC/104 computer and a TS-POE100, the only required cable/connection is the POE ethernet cable, which must include network signals and DC power in the same lines. Connect it to the TS-POE100 RJ45 connector.

Power can be either on the spare pairs or on the data pairs of the 8-lines network cable. The power level that must be found at the network cable is 48VDC @ 0.35A. If the TS-POE100 detects valid POE signature and classification stages, it will transmit regulated 5VDC to the PC/104 bus, powering up the other boards (peripherals and computers) connected to it.

The on-board green LED named LED 5V will become on in case the TS-POE100 detects a valid POE power source. Also, there are on-board LEDs for the MAC, indicating speed of the link and network activity on the cable.

The TS-POE100 can provide up to 12W of power (2.4Amp @ 5VDC) – this is Class 3 POE implementation.

SOFTWARE SUPPORT

The register map of ASIX AX88796B ethernet chip is NE2000 compatible, so driver support is straight-forward. Technologic Systems provides a Linux driver for the ASIX Ethernet interface suitable for both Kernel versions 2.4 and 2.6. The Linux driver provided detects jumper selection, automatically configuring IRQ and IO parameters. In case one wants to skip this feature, the “mem” and “irq” parameters are available to set up I/O base address and IRQ line, respectively.

To load the driver using the auto-detection feature and Kernel 2.4, use:

```
# insmod -f ax88796b.o
```

To load the driver using the parameters and Kernel 2.4 for ARM, with a board with only the IRQ5 jumper ON, use:

```
# insmod -f ax88796b.o mem=0x100 irq=33
```

Notice that in some systems the kernel module “crc32.o” must be loaded before the TS-POE100 driver.

In addition, Technologic Systems provides Linux tools to manage the sleep-mode and Wake-on-LAN functions. A Linux tool to program the MAC address on the EEPROM chip is also provided. Contact Technologic Systems for further information regarding software support for the TS-POE100.

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DOCUMENT HISTORY

11.26.2007 – CREATED